

COMPAL CONFIDENTIAL

MODEL NAME : EDA70

PCB NO : LA-H281P

BOM P/N : 451AG431L01

GPIO MAP: X10_CFLH_GPIO map Rev1.5_20181224

Vinafix.com

WHITEHAVEN MLK 17

Coffee Lake-R type (2 chip)

REV : 1.0(A00)

2019.4.10

Pop Component

EMI@, RF@, ESD@ : EMI/ESD/RF part POP

CONN@ : Connector Component

XDP@ : Total debug Component (pop them until ST)

NDS3@ : non Deep sleep support

eSPI@ : eSPI interface

RTD3@ : TBT RTD3 support

@ : Nopop Component

@EMI@, @RF@, @ESD@ : EMI/ESD/RF part nopop

DS3@ : Deep sleep support

LPC@ : LPC interface

NRTD3@ : non TBT RTD3 support

Layout Dell logo



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REV: X00
PWB: XXXXX
DATE: 1707-03

PCB 26K LA-H281P REV0 MB AR 3

Part Number	Description
DA80004E000	PCB 26K LA-H281P REV0 MB AR 3

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		1.0	
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POWER STATES

Signal State	SLP S3#	SLP S4#	SLP S5#	S4 STATE#	ALWAYS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	ON	ON	ON
S3 (Suspend to RAM) / M1	LOW	HIGH	HIGH	HIGH	ON	OFF	OFF
S4 (Suspend to DISK) / M1	LOW	LOW	HIGH	LOW	ON	OFF	OFF
S5 (SOFT OFF) / M1	LOW	LOW	LOW	LOW	ON	OFF	OFF
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	HIGH	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	ON	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	ON	OFF	OFF

PM TABLE

State	power plane	+PWR_SRC +5V_ALW +3.3V_ALW +3.3V_ALW2 +3.3V_ALW_DSW +3.3V_ALW_PCH +3.3V_RTC_LDO +1.8V_ALW +1.0V_PRIM +1.8V_PRIM	+3.3V_SUS +1.2V_MEM +2.5V_MEM +1.0V_VCCST	+5V_RUN +3.3V_RUN +1.2V_RUN +3.3V_DGFF +5V_DGFF +DGFF_PWR_SRC +0.675V_DDR_VTT	(M-OFF) +VCC_CORE +VCC_GT +VCC_IO +VCC_SA +1.0V_VCCSTG +1.8V_RUN
S0		ON	ON	ON	ON
S3		ON	ON	OFF	OFF
S5 S4/AC		ON	OFF	OFF	OFF
S5 S4/AC don't exist		OFF	OFF	OFF	OFF

PCH	USB2 PORT#	DESTINATION
	1	JUSB1
	2	JUSB2
	3	JUSB3
	4	Cypress PD
	5	Cypress PD
	6	NA
	7	NA
	8	M.2 Slot-2 (WWAN/LTE)
	9	17" NA/ 15" Touch screen
	10	USH
	11	Camera
	12	NA
	13	NA
	14	M.2 Slot-1 (BT)
USH	0	BIO
	1	NA

PCI EXPRESS	DESTINATION
PORT 1~4	TBT-Titan Ridge
PORT 5	10/100/1G LOM
PORT 6	MMI(Card reader)
PORT 7	M.2 Slot-1 (WLAN/Wigig)
PORT 8	M.2 Slot-2 (WWAN/LTE)
PORT9~12	SLOT3 SSD 2280/ Optane
PORT13~16	SLOT6 SSD 2280/NVME
PORT17~20	SLOT4 SSD 2280/ Optane
PORT21~24	SLOT5 PCIE only 2280/ Optane

Layer No.	Name	Er for polar	DF	Material	Thickness (Material SPEC.) Unit : mil	Thickness (Actuality) Unit : mil
	S/M	3.7	0.047	SolderMask	HF GA-HF-15	0.80
1	Top	3.7	0.018	Copper foil	Hoz+plating	1.55
				Prepreg	pp1086LR	2.55
2	GND/PWR	3.8	0.0153	Copper foil	1oz	1.30
				Core	4mil core	4.00
3	IN1	3.8	0.017	Copper foil	Hoz	0.65
				Prepreg	pp2116HR	4.70
4	GND/PWR	3.7	0.0186	Copper foil	Hoz	0.65
				Core	3mil core	3.00
5	IN2	3.8	0.017	Copper foil	Hoz	0.65
				Prepreg	pp2116HR	4.30
6	GND/PWR	3.7	0.0186	Copper foil	2oz	2.60
				Core	3mil core	3.00
7	GND/PWR	3.8	0.017	Copper foil	2oz	2.60
				Prepreg	pp2116HR	4.30
8	IN3	3.7	0.0186	Copper foil	Hoz	0.65
				Core	3mil core	3.00
9	GND/PWR	3.8	0.017	Copper foil	Hoz	0.65
				Prepreg	pp2116HR	4.70
10	IN4	3.8	0.0153	Copper foil	Hoz	0.65
				Core	4mil core	4.00
11	GND/PWR	3.7	0.018	Copper foil	1oz	1.30
				Prepreg	pp1086LR	2.55
12	Bottom	3.7	0.047	SolderMask	Hoz+plating	1.55
						0.80
Overall Thickness (1.45mm ± 10%)					56.50000	1.4351

USB3.0	DESTINATION
Port 1	JUSB1
Port 2	M.2 Slot-2 (WWAN/LTE)
Port 3	JUSB2
Port 4	JUSB3
Port 5	NA
Port 6	NA

SATA	DESTINATION
SATA 0B	SLOT6 SSD
SATA 1A	SLOT3 SSD
SATA 2	NA
SATA 3	NA
SATA 4	SLOT4 SSD/HDD
SATA 5	NA

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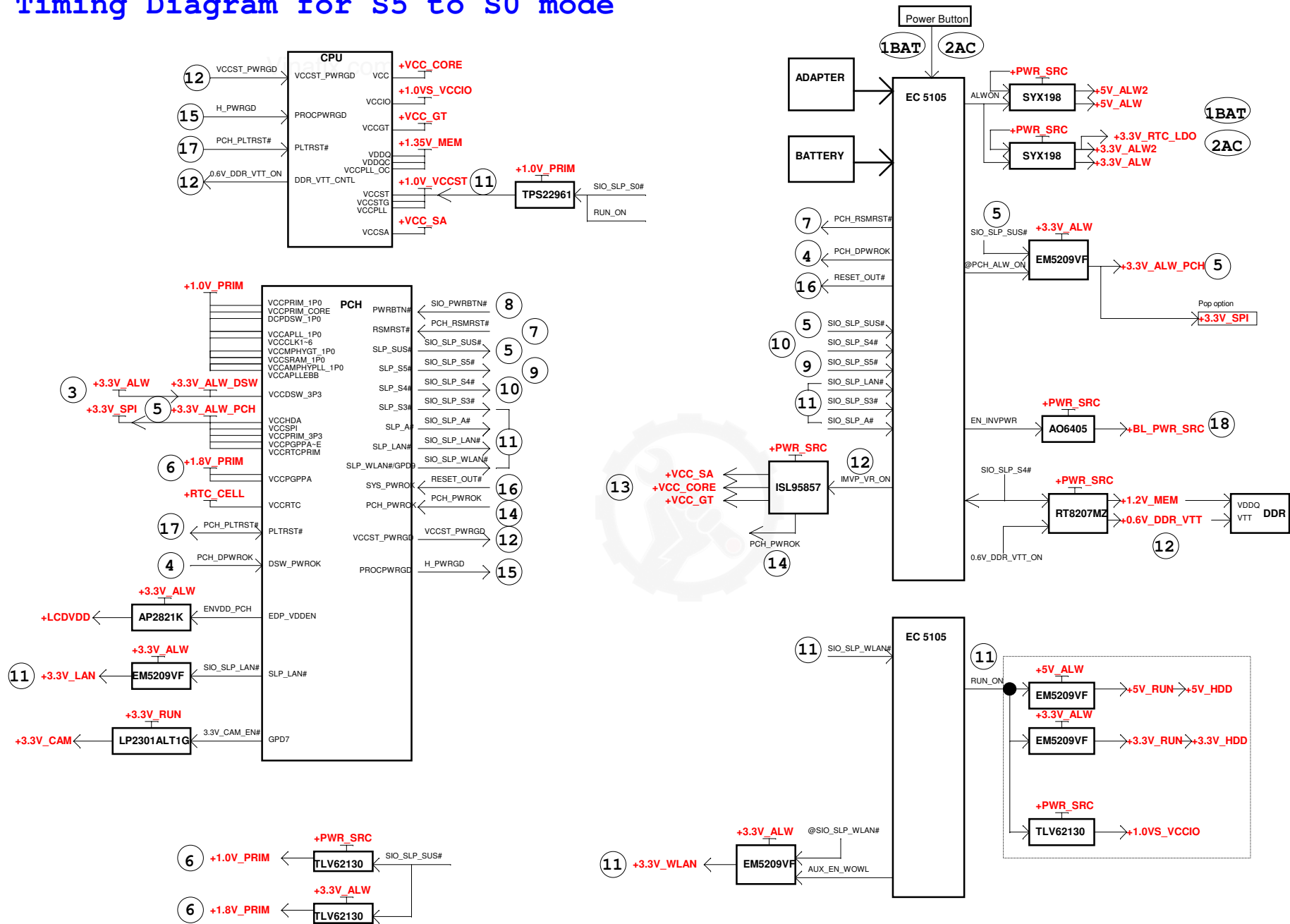
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Notes List

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Timing Diagram for S5 to S0 mode



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Title
Power Sequence

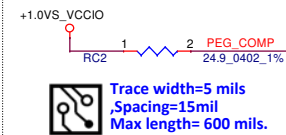
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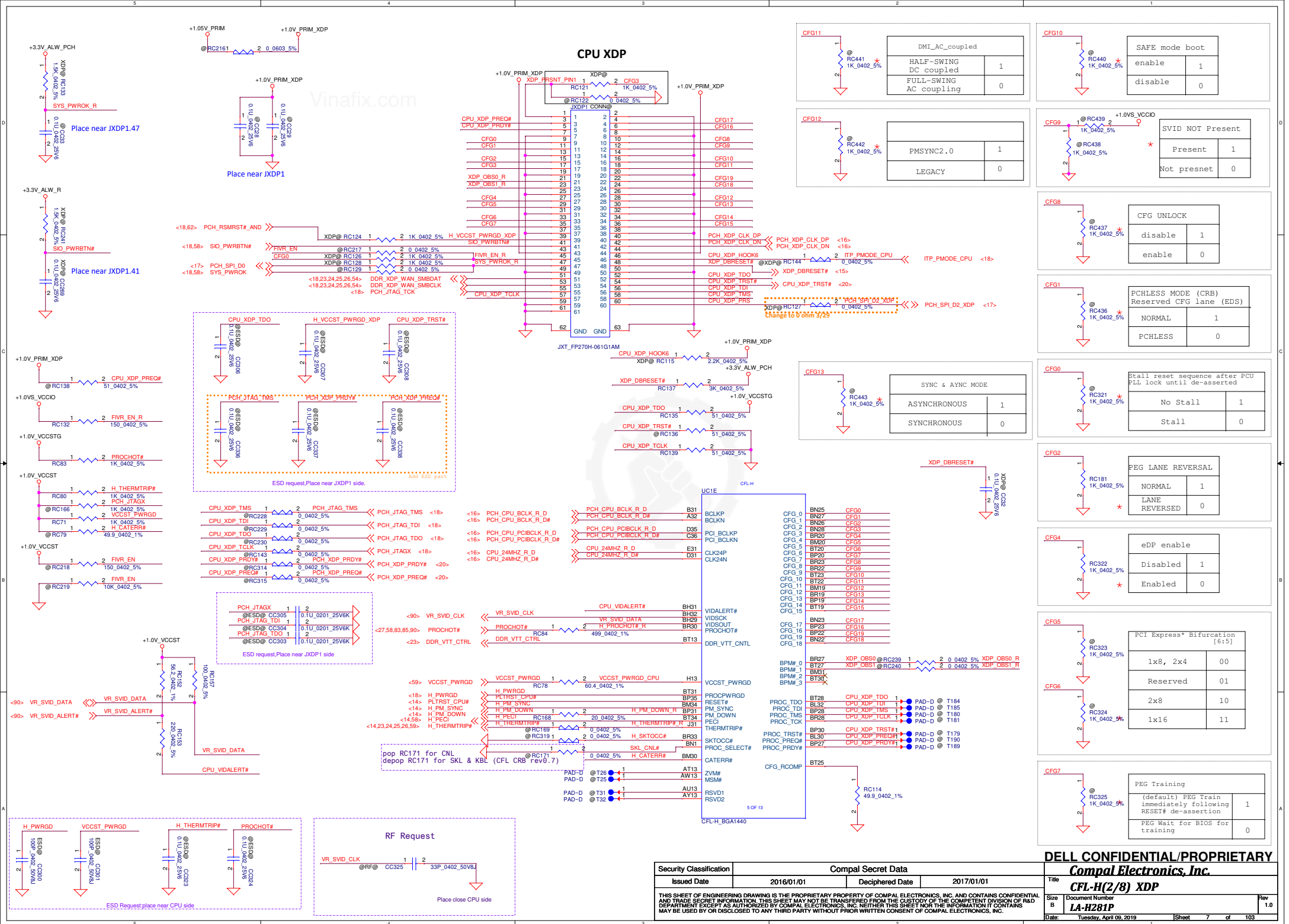


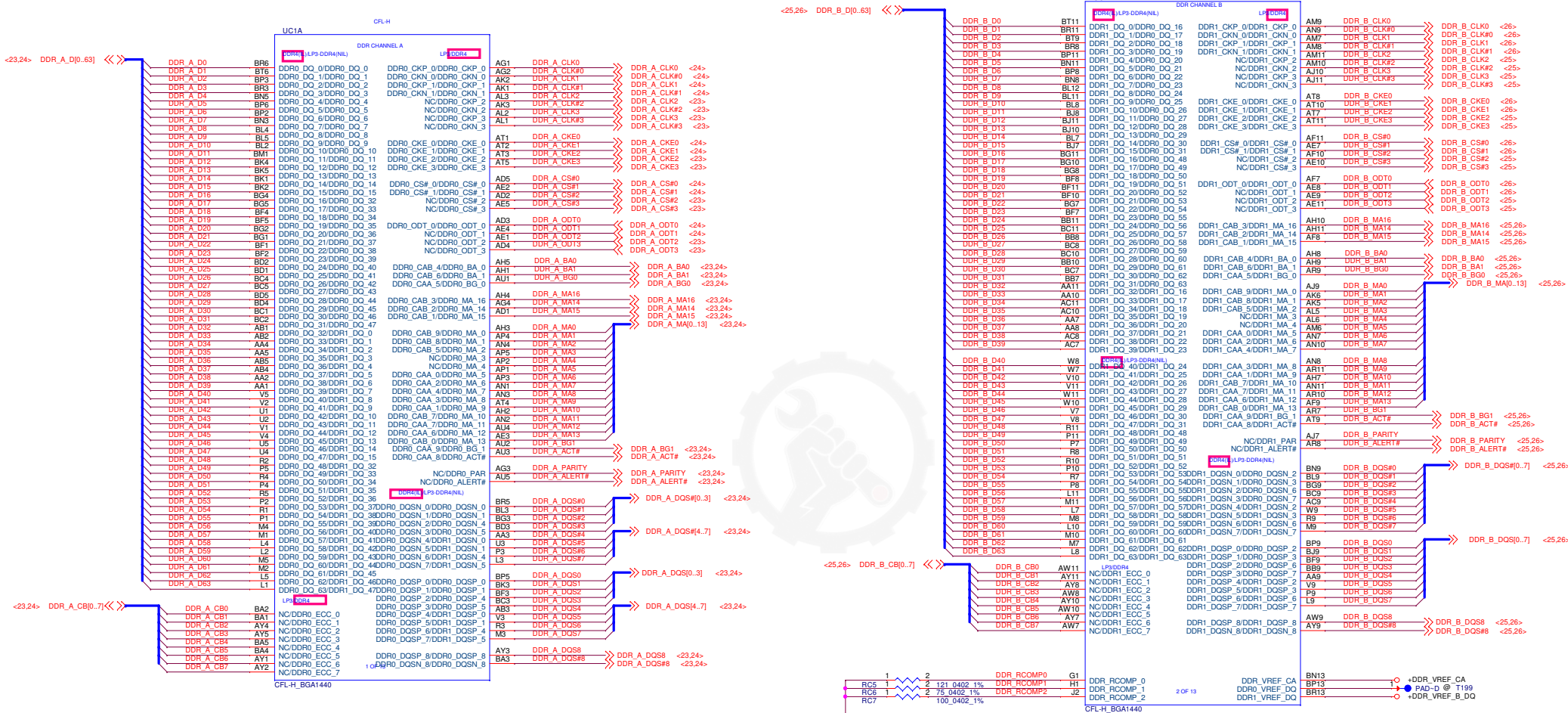
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<15>	DMI_CRX_PTX_N0	>>	DMI_CRX_PTX_N0	E8	DMI_RXN_0	DMI_TXN_0	A8	DMI_CTX_PRX_N0	>>	DMI_CTX_PRX_N0	<15>
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<15>	DMI_CRX_PTX_N1	>>	DMI_CRX_PTX_N1	E6	DMI_RXN_1	DMI_TXN_1	B6	DMI_CTX_PRX_N1	>>	DMI_CTX_PRX_N1	<15>
<15>	DMI_CRX_PTX_P2	>>	DMI_CRX_PTX_P2	D5	DMI_RXP_2	DMI_TXP_2	B5	DMI_CTX_PRX_P2	>>	DMI_CTX_PRX_P2	<15>
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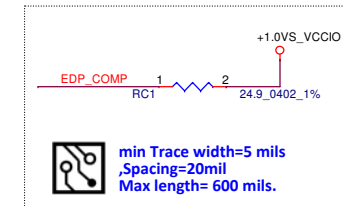
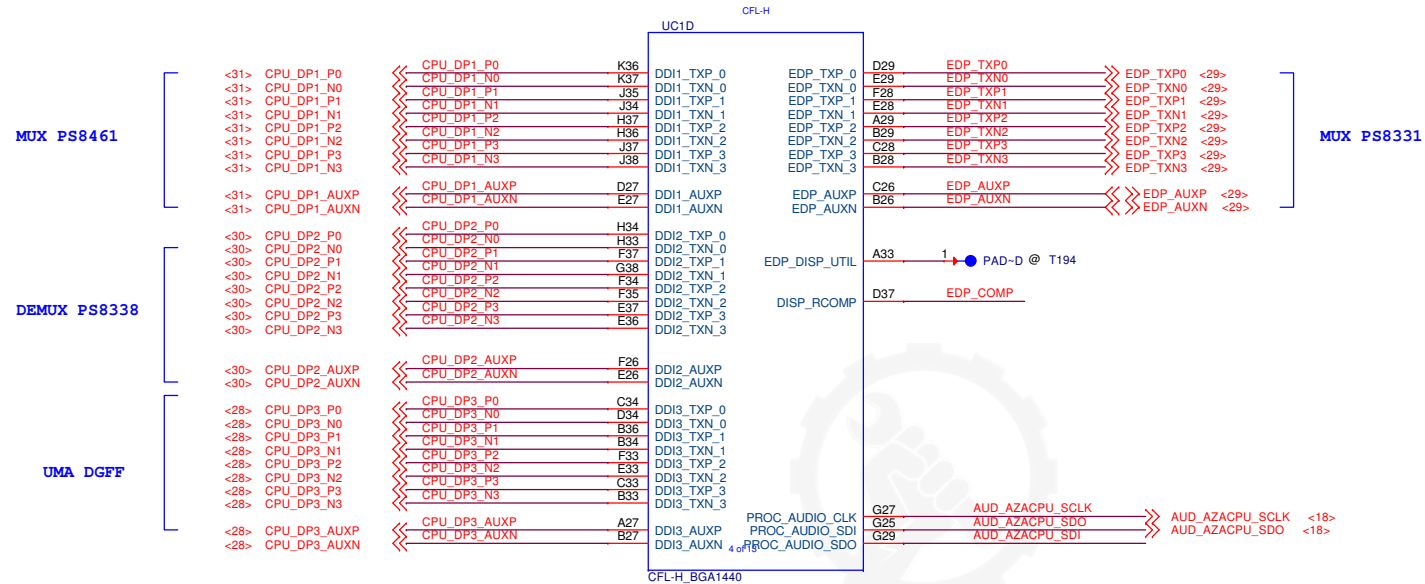
CFL-H_BGA1440

CPL-H

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PEG_CRX_GTX_P8	E18	PEG_RXP_7	PEG_TXP_7	B18	PEG_CTX_GRX_P8	CC48	1	2	0.22U	0402	16V7K	PEG_CTX_C_GRX_P8
PEG_CRX_GTX_N8	F18	PEG_RXN_7	PEG_TXN_7	C18	PEG_CTX_GRX_N8	CC49	1	2	0.22U	0402	16V7K	PEG_CTX_C_GRX_N8
PEG_CRX_GTX_P7	D17	PEG_RXP_8	PEG_TXP_8	A17	PEG_CTX_GRX_P7	CC50	1	2	0.22U	0402	16V7K	PEG_CTX_C_GRX_P7
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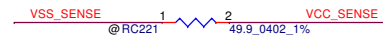
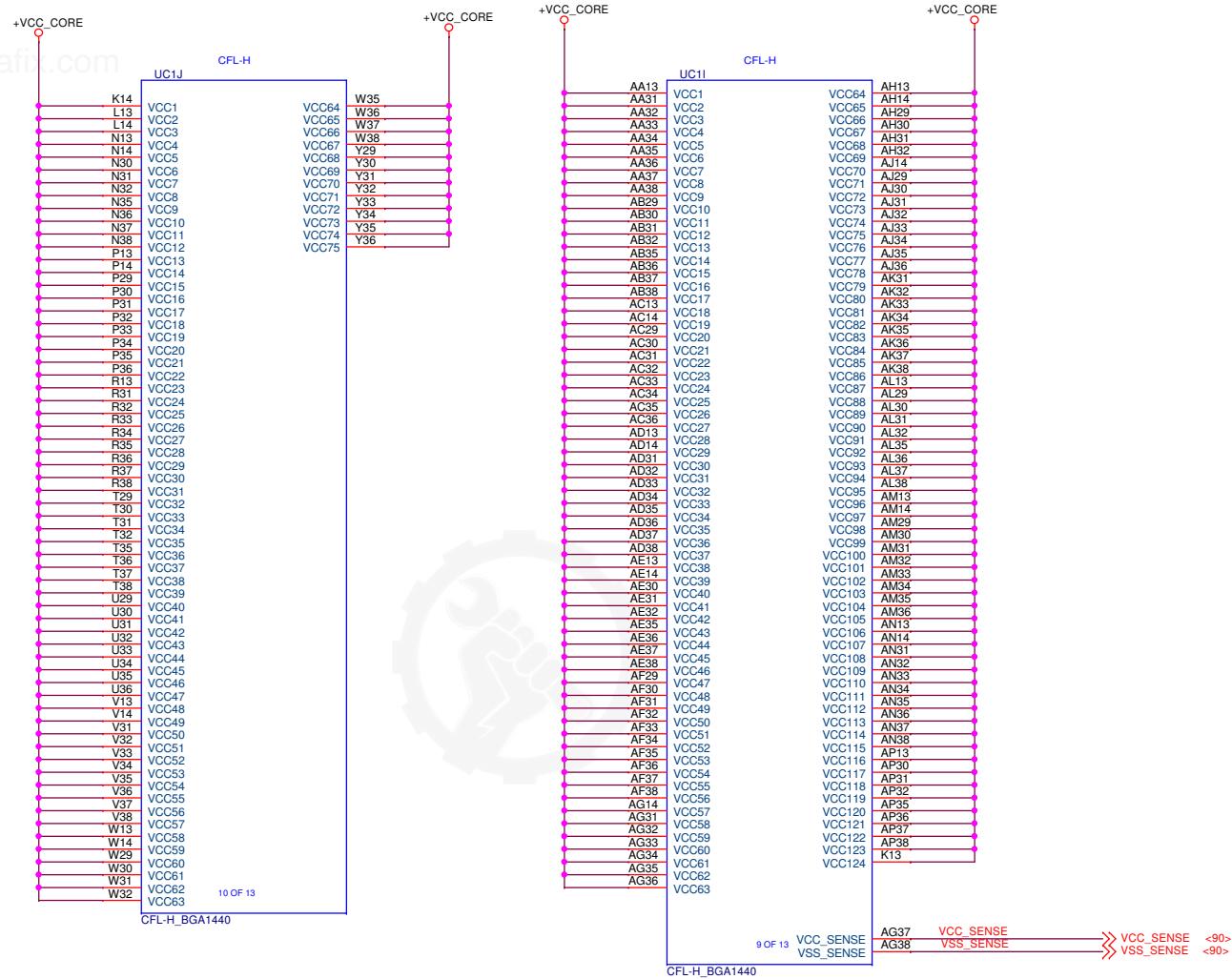






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CFL-H		
UC1F		
A10	VSS_1	VSS_82
A16	VSS_2	VSS_83
A18	VSS_3	VSS_84
A20	VSS_4	VSS_85
A22	VSS_5	VSS_86
A24	VSS_6	VSS_87
A26	VSS_7	VSS_88
A28	VSS_8	VSS_89
A30	VSS_9	VSS_90
A6	VSS_10	VSS_91
A9	VSS_11	VSS_92
AA12	VSS_12	VSS_93
AA29	VSS_13	VSS_94
AA30	VSS_14	VSS_95
AB33	VSS_15	VSS_96
AB34	VSS_16	VSS_97
AB6	VSS_17	VSS_98
AC1	VSS_18	VSS_99
AC12	VSS_19	VSS_100
AC2	VSS_20	VSS_101
AC3	VSS_21	VSS_102
AC37	VSS_22	VSS_103
AC38	VSS_23	VSS_104
AC4	VSS_24	VSS_105
AC5	VSS_25	VSS_106
AC6	VSS_26	VSS_107
AD10	VSS_27	VSS_108
AD11	VSS_28	VSS_109
AD12	VSS_29	VSS_110
AD29	VSS_30	VSS_111
AD30	VSS_31	VSS_112
AD6	VSS_32	VSS_113
AD8	VSS_33	VSS_114
AD9	VSS_34	VSS_115
AE33	VSS_35	VSS_116
AE34	VSS_36	VSS_117
AE6	VSS_37	VSS_118
AF1	VSS_38	VSS_119
AF12	VSS_39	VSS_120
AF13	VSS_40	VSS_121
AF14	VSS_41	VSS_122
AF2	VSS_42	VSS_123
AF3	VSS_43	VSS_124
AF4	VSS_44	VSS_125
AG10	VSS_45	VSS_126
AG11	VSS_46	VSS_127
AG13	VSS_47	VSS_128
AG29	VSS_48	VSS_129
AG30	VSS_49	VSS_130
AG6	VSS_50	VSS_131
AG7	VSS_51	VSS_132
AG8	VSS_52	VSS_133
AH12	VSS_53	VSS_134
AH33	VSS_54	VSS_135
AH34	VSS_55	VSS_136
AH35	VSS_56	VSS_137
AH36	VSS_57	VSS_138
AH6	VSS_58	VSS_139
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AJ13	VSS_60	VSS_141
AJ2	VSS_61	VSS_142
AJ3	VSS_62	VSS_143
AJ37	VSS_63	VSS_144
AJ38	VSS_64	VSS_145
AJ4	VSS_65	VSS_146
AJ5	VSS_66	VSS_147
AJ6	VSS_67	VSS_148
W4	VSS_68	VSS_149
W5	VSS_69	VSS_150
Y10	VSS_70	VSS_151
Y11	VSS_71	VSS_152
Y13	VSS_72	VSS_153
Y14	VSS_73	VSS_154
Y37	VSS_74	VSS_155
Y38	VSS_75	VSS_156
Y7	VSS_76	VSS_157
Y8	VSS_77	VSS_158
Y9	VSS_78	VSS_159
AK29	VSS_79	VSS_160
AK30	VSS_80	VSS_161
	VSS_81	VSS_162

CFL-H_BGA1440

CFL-H		
UC1G		
AW5	VSS_163	VSS_244
AY12	VSS_164	VSS_245
AY33	VSS_165	VSS_246
AY34	VSS_166	VSS_247
B9	VSS_167	VSS_248
BA10	VSS_168	VSS_249
BA11	VSS_169	VSS_250
BA12	VSS_170	VSS_251
BA37	VSS_171	VSS_252
BA38	VSS_172	VSS_253
BA6	VSS_173	VSS_254
BA7	VSS_174	VSS_255
BA8	VSS_175	VSS_256
BA9	VSS_176	VSS_257
BB1	VSS_177	VSS_258
BB12	VSS_178	VSS_259
BB2	VSS_179	VSS_260
BB29	VSS_180	VSS_261
BB3	VSS_181	VSS_262
BB30	VSS_182	VSS_263
BB4	VSS_183	VSS_264
BB5	VSS_184	VSS_265
BB6	VSS_185	VSS_266
BC12	VSS_186	VSS_267
BC13	VSS_187	VSS_268
BC14	VSS_188	VSS_269
BC33	VSS_189	VSS_270
BC34	VSS_190	VSS_271
BC6	VSS_191	VSS_272
BD10	VSS_192	VSS_273
BD11	VSS_193	VSS_274
BD12	VSS_194	VSS_275
BD37	VSS_195	VSS_276
BD6	VSS_196	VSS_277
BD7	VSS_197	VSS_278
BD8	VSS_198	VSS_279
BD9	VSS_199	VSS_280
BE1	VSS_200	VSS_281
BE2	VSS_201	VSS_282
BE29	VSS_202	VSS_283
BE3	VSS_203	VSS_284
BE30	VSS_204	VSS_285
BE4	VSS_205	VSS_286
BE5	VSS_206	VSS_287
BE6	VSS_207	VSS_288
BF12	VSS_208	VSS_289
BF33	VSS_209	VSS_290
BF34	VSS_210	VSS_291
BF6	VSS_211	VSS_292
BG12	VSS_212	VSS_293
BG13	VSS_213	VSS_294
BG14	VSS_214	VSS_295
BG37	VSS_215	VSS_296
BG38	VSS_216	VSS_297
BG6	VSS_217	VSS_298
BH1	VSS_218	VSS_299
BH10	VSS_219	VSS_300
BH11	VSS_220	VSS_301
BH12	VSS_221	VSS_302
BH14	VSS_222	VSS_303
BH2	VSS_223	VSS_304
BH3	VSS_224	VSS_305
BH4	VSS_225	VSS_306
BH5	VSS_226	VSS_307
BH6	VSS_227	VSS_308
BH7	VSS_228	VSS_309
BH8	VSS_229	VSS_310
BH9	VSS_230	VSS_311
I2	VSS_231	VSS_312
I3	VSS_232	VSS_313
I33	VSS_233	VSS_314
I34	VSS_234	VSS_315
T4	VSS_235	VSS_316
T5	VSS_236	VSS_317
T7	VSS_237	VSS_318
T8	VSS_238	VSS_319
T9	VSS_239	VSS_320
U37	VSS_240	VSS_321
U38	VSS_241	VSS_322
BU12	VSS_242	VSS_323
BU14	VSS_243	VSS_324

CFL-H_BGA1440

CFL-H		
UC1H		
BN4	VSS_325	VSS_409
BN7	VSS_326	VSS_410
BP12	VSS_327	VSS_411
BP14	VSS_328	VSS_412
BP18	VSS_329	VSS_413
BP21	VSS_330	VSS_414
BP24	VSS_331	VSS_415
BP25	VSS_332	VSS_416
BP26	VSS_333	VSS_417
BP29	VSS_334	VSS_418
BP33	VSS_335	VSS_419
BP34	VSS_336	VSS_420
BP7	VSS_337	VSS_421
BR12	VSS_338	VSS_422
BR14	VSS_339	VSS_423
BR18	VSS_340	VSS_424
BR21	VSS_341	VSS_425
BR24	VSS_342	VSS_426
BR25	VSS_343	VSS_427
BR26	VSS_344	VSS_428
BR29	VSS_345	VSS_429
BR34	VSS_346	VSS_430
BR36	VSS_347	VSS_431
BR7	VSS_348	VSS_432
BT12	VSS_349	VSS_433
BT14	VSS_350	VSS_434
BT18	VSS_351	VSS_435
BT21	VSS_352	VSS_436
BT24	VSS_353	VSS_437
BT26	VSS_354	VSS_438
BT29	VSS_355	VSS_439
BT32	VSS_356	VSS_440
BT5	VSS_357	VSS_441
C11	VSS_358	VSS_442
C13	VSS_359	VSS_443
C15	VSS_360	VSS_444
C17	VSS_361	VSS_445
C19	VSS_362	VSS_446
C21	VSS_363	VSS_447
C23	VSS_364	VSS_448
C25	VSS_365	VSS_449
C27	VSS_366	VSS_450
C29	VSS_367	VSS_451
C31	VSS_368	VSS_452
C37	VSS_369	VSS_453
C5	VSS_370	VSS_454
C8	VSS_371	VSS_455
C9	VSS_372	VSS_456
D10	VSS_373	VSS_457
D12	VSS_374	VSS_458
D14	VSS_375	VSS_459
D16	VSS_376	VSS_460
D18	VSS_377	VSS_461
D20	VSS_378	VSS_462
D22	VSS_379	VSS_463
D24	VSS_380	VSS_464
D26	VSS_381	VSS_465
D28	VSS_382	VSS_466
D3	VSS_383	VSS_467
D30	VSS_384	VSS_468
D33	VSS_385	VSS_469
D6	VSS_386	VSS_470
D9	VSS_387	VSS_471
E34	VSS_388	VSS_472
E35	VSS_389	VSS_473
E38	VSS_390	VSS_474
E4	VSS_391	VSS_475
E9	VSS_392	VSS_476
N3	VSS_393	VSS_477
N33	VSS_394	VSS_478
N34	VSS_395	VSS_479
N4	VSS_396	
N5	VSS_397	VSS_A3
N6	VSS_398	VSS_A34
N7	VSS_399	VSS_A4
N8	VSS_400	VSS_B3
N9	VSS_401	VSS_B37
P12	VSS_402	VSS_BR38
P37	VSS_403	VSS_BT3
M14	VSS_404	VSS_BT35
M6	VSS_405	VSS_BT36
N1	VSS_406	VSS_BT4
F11	VSS_407	VSS_C2
F13	VSS_408	VSS_D38

CFL-H_BGA1440

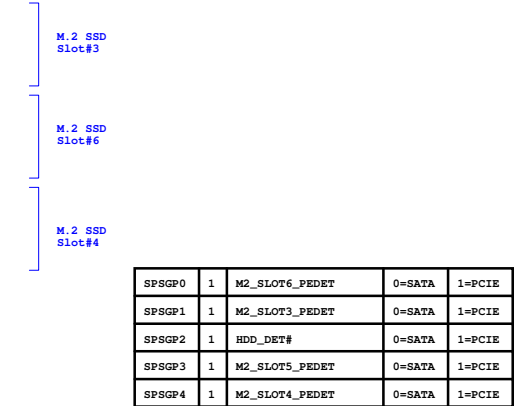
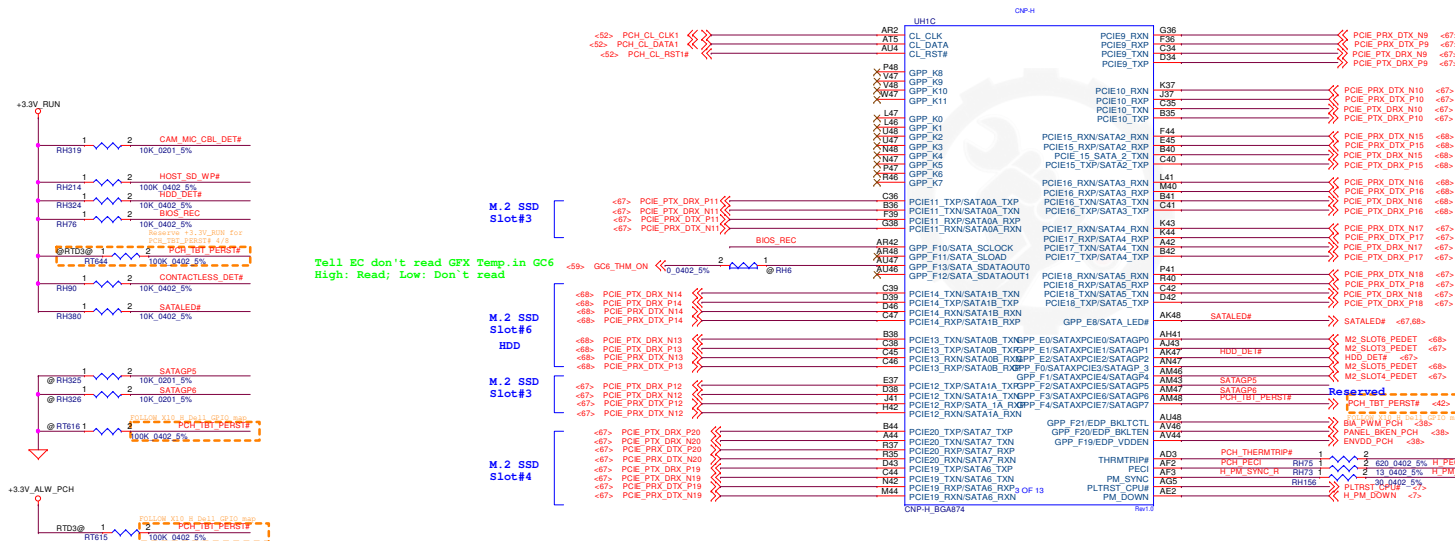
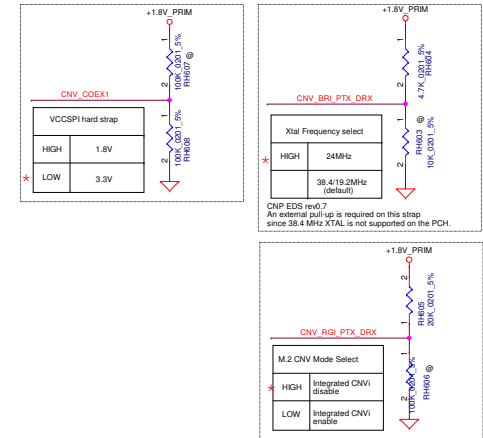
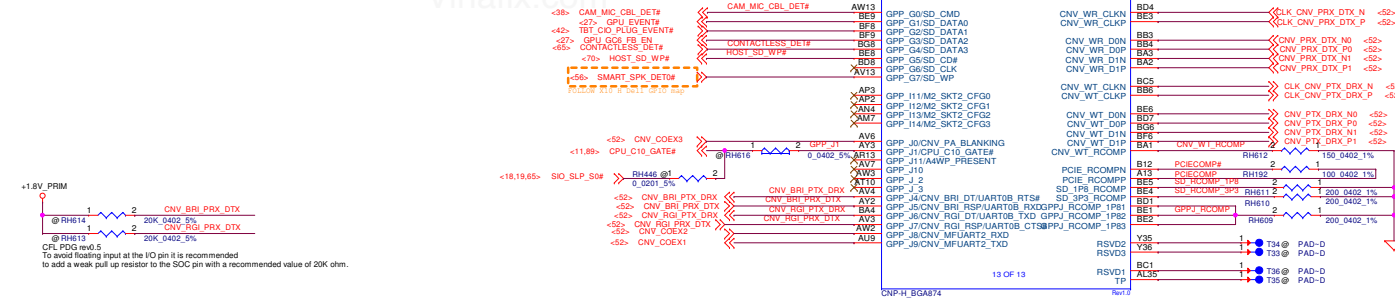
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CFL-H(8/8) GND

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				Date:	Tuesday, April 09, 2019
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Rev 1.0



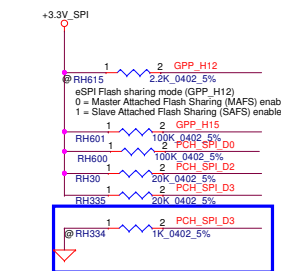
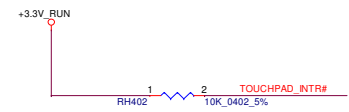
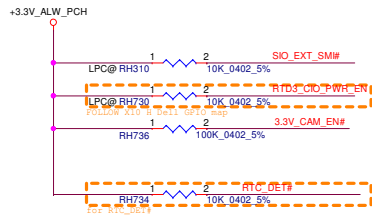
SPSGP0	1	M2_SLOT6_PEDDET	0=SATA 1=PCIE
SPSGP1	1	M2_SLOT3_PEDDET	0=SATA 1=PCIE
SPSGP2	1	HDD_DET#	0=SATA 1=PCIE
SPSGP3	1	M2_SLOT5_PEDDET	0=SATA 1=PCIE
SPSGP4	1	M2_SLOT4_PEDDET	0=SATA 1=PCIE

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CNP-H(1/9) PCIE,CNV

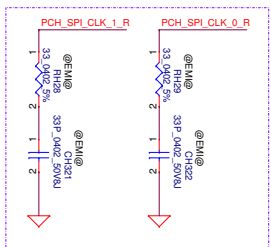
Security Classification	Compal Secret Data		Issue Date	Deciphered Date	2017/01/01
Document Number	LA-H281P		Size	1.0	Rev
Date:	Tuesday, April 05, 2017		Sheet	14	of 103



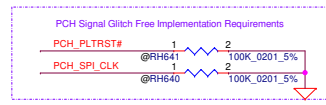
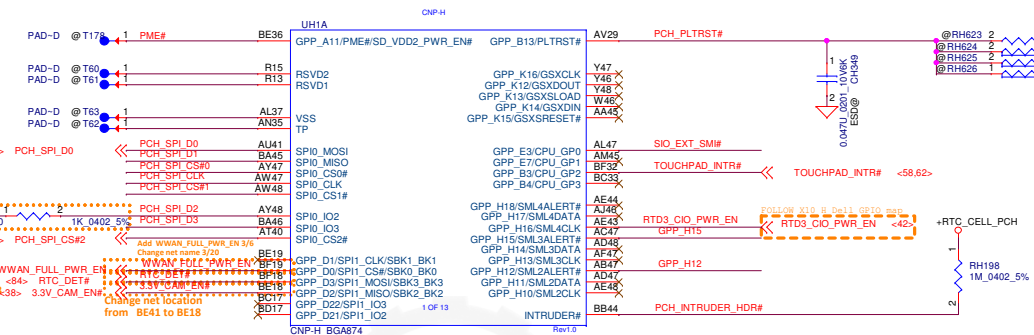
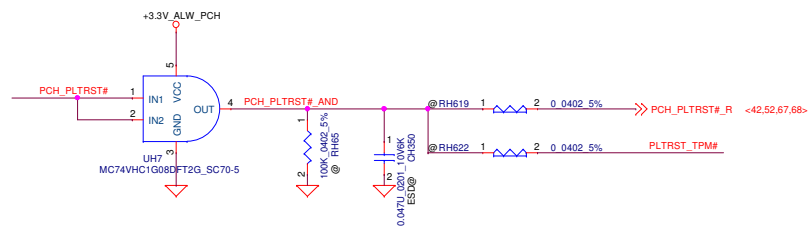
CFL-H PDG rev0.7
pop 20K for SPD_IO2/3
CNL: PCH EDS rev0.5
Reserved External pull-up is required. Recommend 100K if pulled up to 3.3V

9/5 MOW
Option 1: Implement a 1 kOhm pull-down resistor on the signal and de-populate the required 1 kOhm pull-up resistor. In this case, customers must ensure that the SPI flash device on the platform has HOLD functionality disabled by default.
Note that the pull down resistor on SPD_IO3 is only needed for SKL U/Y platforms with ES and SKL 5/H platforms with pre-ES1/ES1 samples.

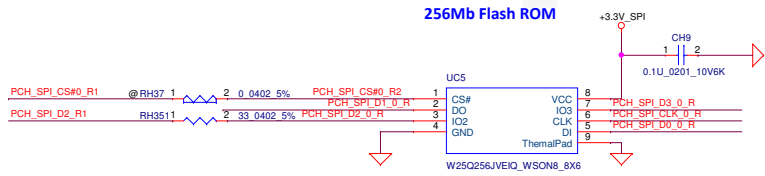
	ESPI	LPC
RH351	33 ohm	15 ohm
RPC1	33 ohm	15 ohm
RH178, RH179, RH181, RH182, RH183, RH184	0 ohm	25 ohm



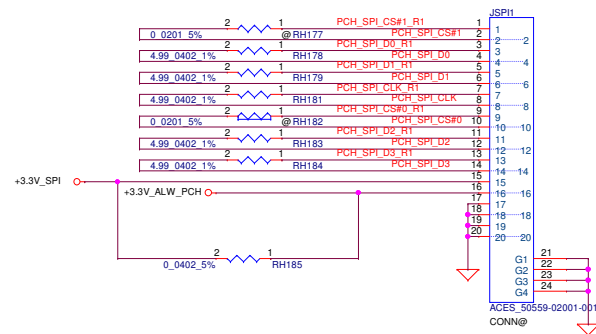
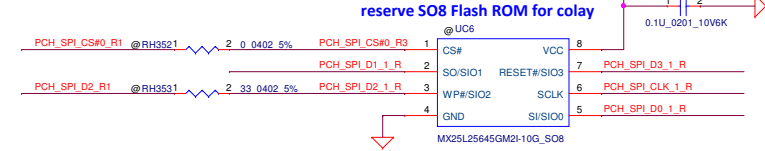
Vinafix.com



256Mb Flash ROM

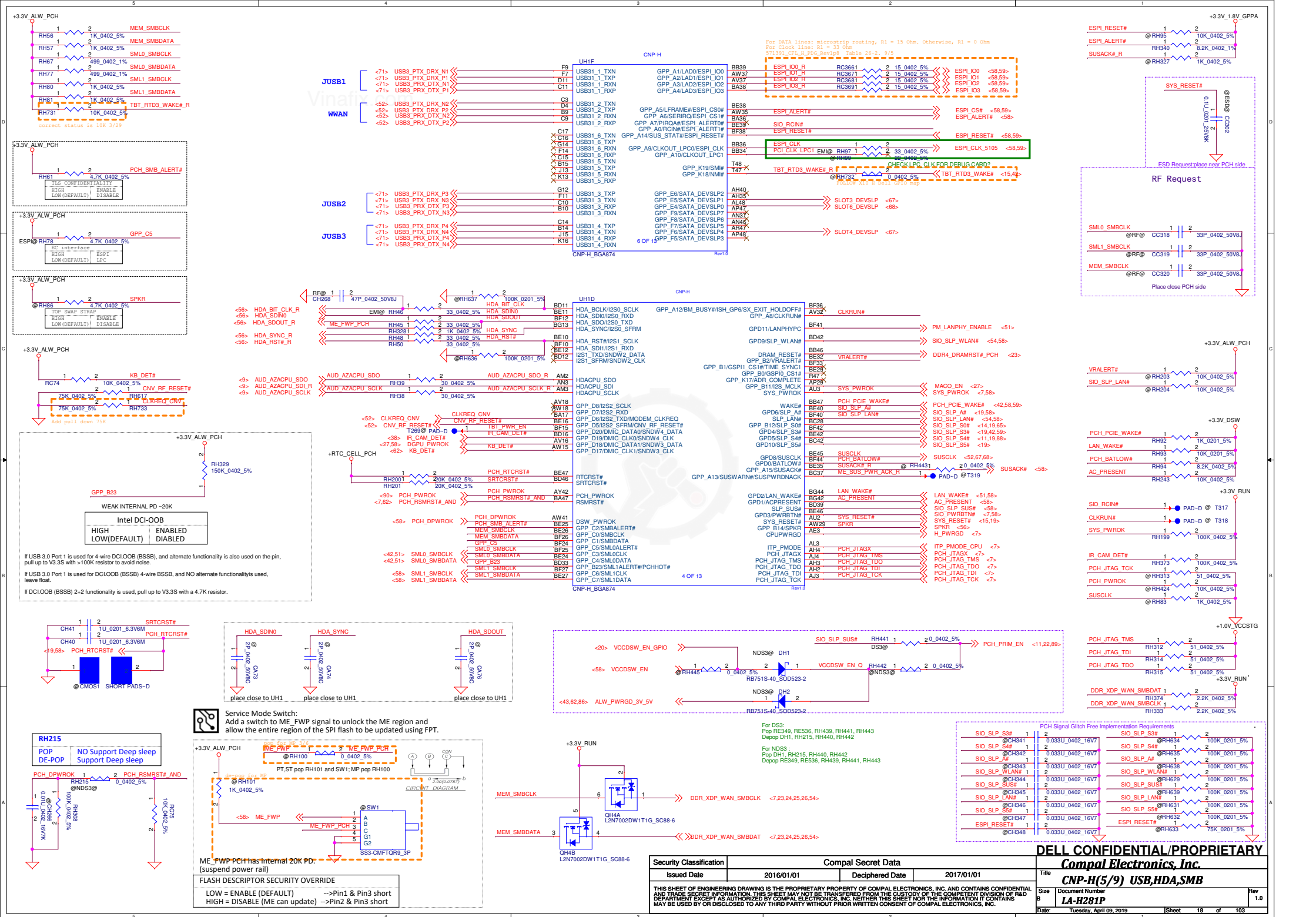


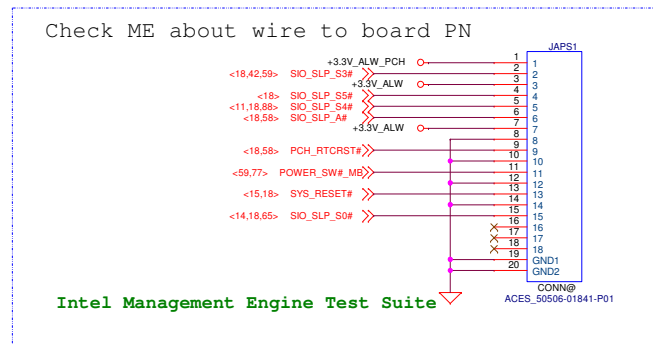
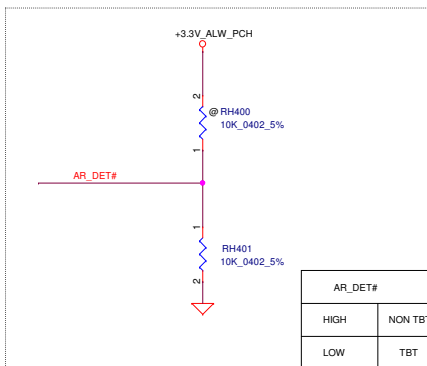
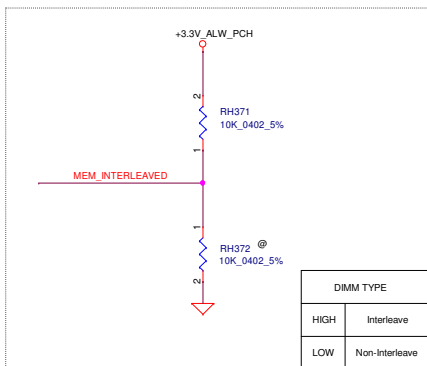
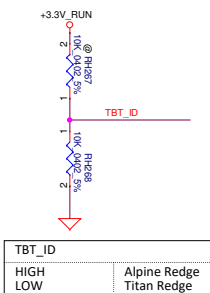
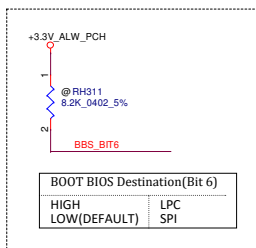
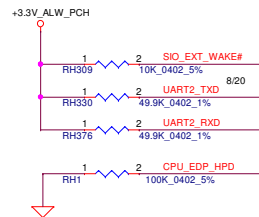
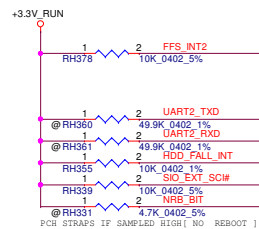
reserve S08 Flash ROM for colay



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CNP-H(4/9) SPI,PLTRST

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			Document Number
			LA-H281P
			Rev 1.0
			Date: Tuesday, April 09, 2019
			Sheet 17 of 103





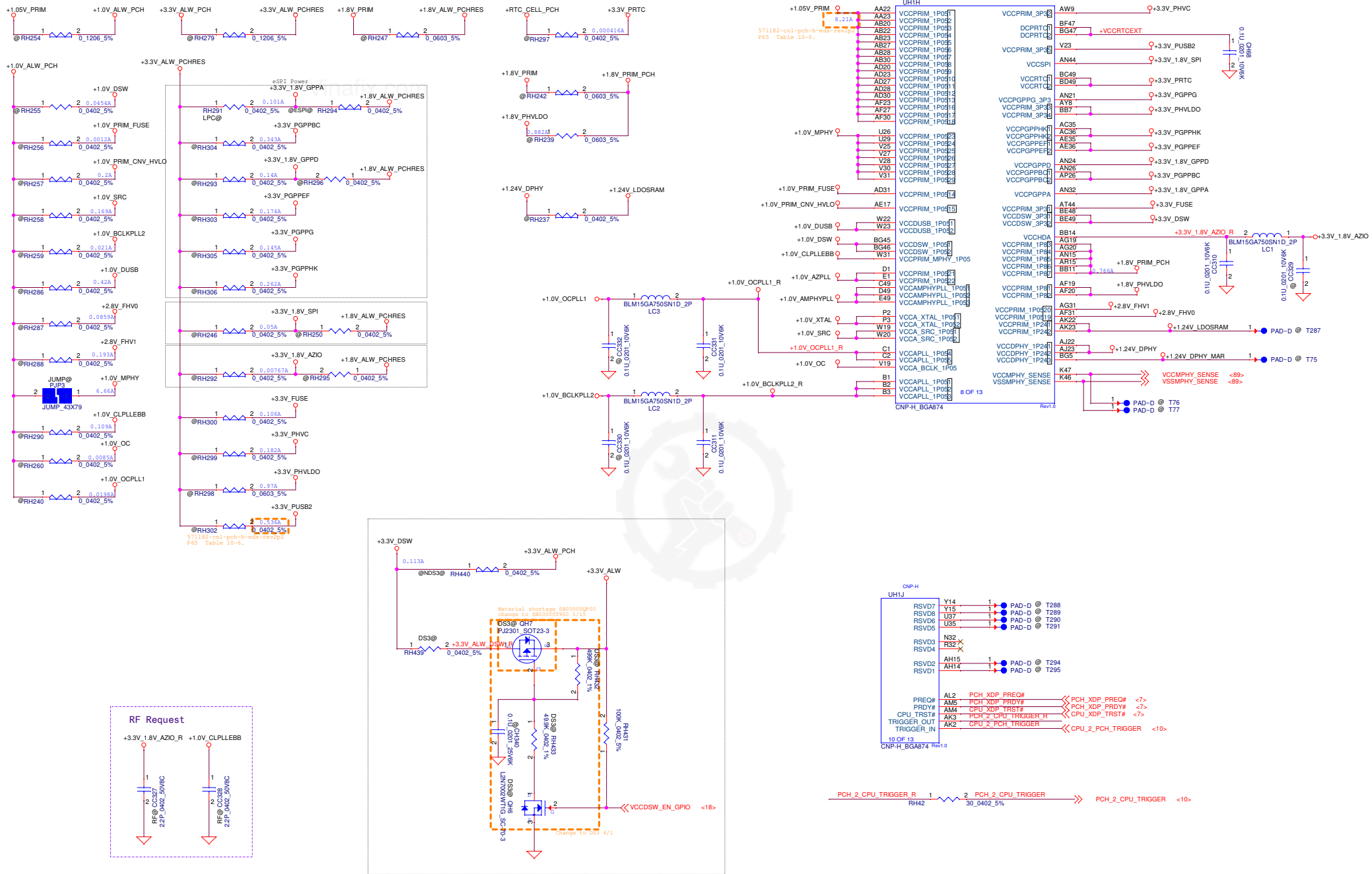
Intel Management Engine Test Suite

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CNP-H(6/9) GPIO,HPD,DDC

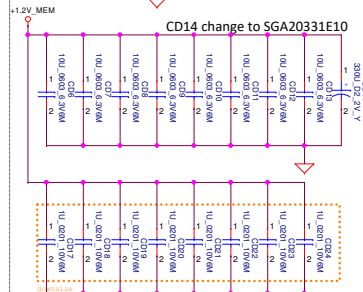
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Issued Date	2016/01/01	Deciphered Date	2017/01/01	Size	Document Number
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Date:	Tuesday, April 09, 2019	Sheet	19	of	103



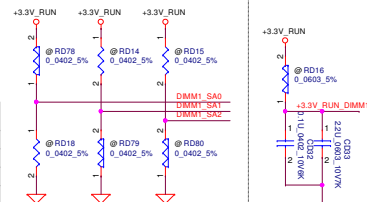
[illegible][illegible][illegible][illegible]

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				Size	Document Number LA-H281P	Rev 1.0
				Date:	Tuesday, April 09, 2019	Sheet 22 of 103

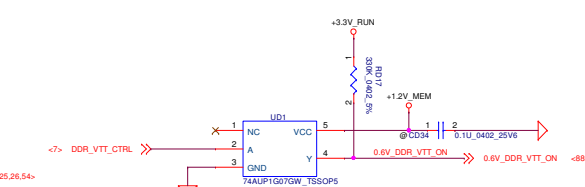
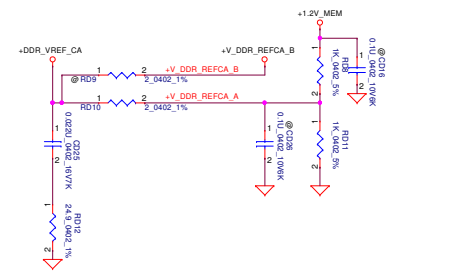
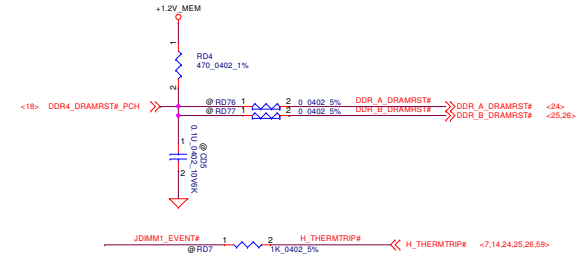
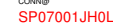
<8.24> DDR_A_CB[0..7] <<>>
 <8.24> DDR_A_DQS#[0..3] <<>>
 <8.24> DDR_A_DQS[0..3] <<>>
 <8.24> DDR_A_DQS#[4..7] <<>>
 <8.24> DDR_A_DQS[4..7] <<>>
 <8.24> DDR_A_D[0..63] <<>>
 <8.24> DDR_A_MA[0..13] <<>>



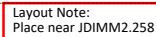
	SA0	SA1	SA2
DIMM2	0	0	0
DIMM4	0	1	0
* DIMM1	1	0	0
DIMM3	1	1	0

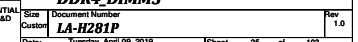


JDIMM1 REV Type H=5.2

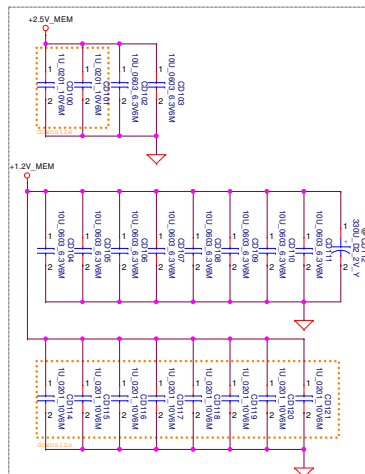


INITIAL &D	Size	Document Number	Rev
	Custom	LA-H281P	1.0
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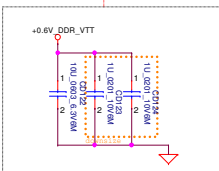




<8.25> DDR_B_C8[0..7] <<>
 <8.25> DDR_B_DQS[0..7] <<>
 <8.25> DDR_B_DQS[0..7] <<>
 <8.25> DDR_B_D[0..63] <<>
 <8.25> DDR_B_MA[0..13] <<>

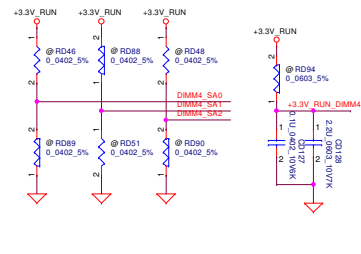


Layout Note:
Place near JDIMM4.258



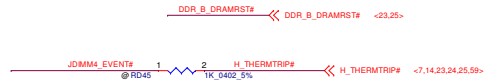
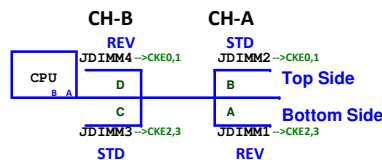
DIMM Select

	SA0	SA1	SA2
DIMM2	0	0	0
DIMM4	0	1	0
DIMM1	1	0	0
DIMM3	1	1	0



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JDIMM4 REV Type H=4



SP07001CY0L

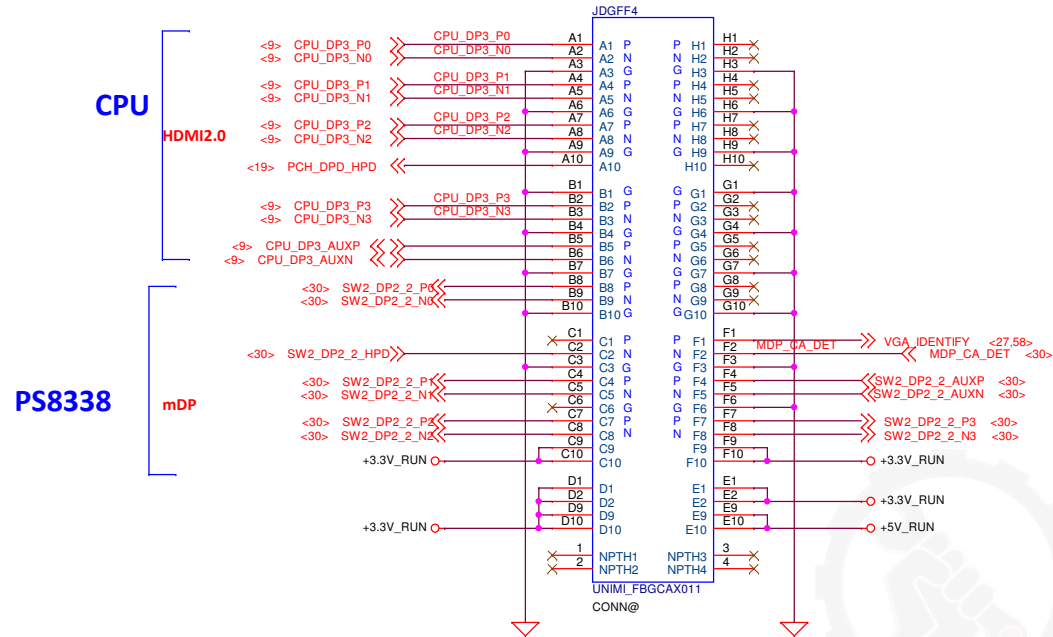
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DDR4_DIMM4

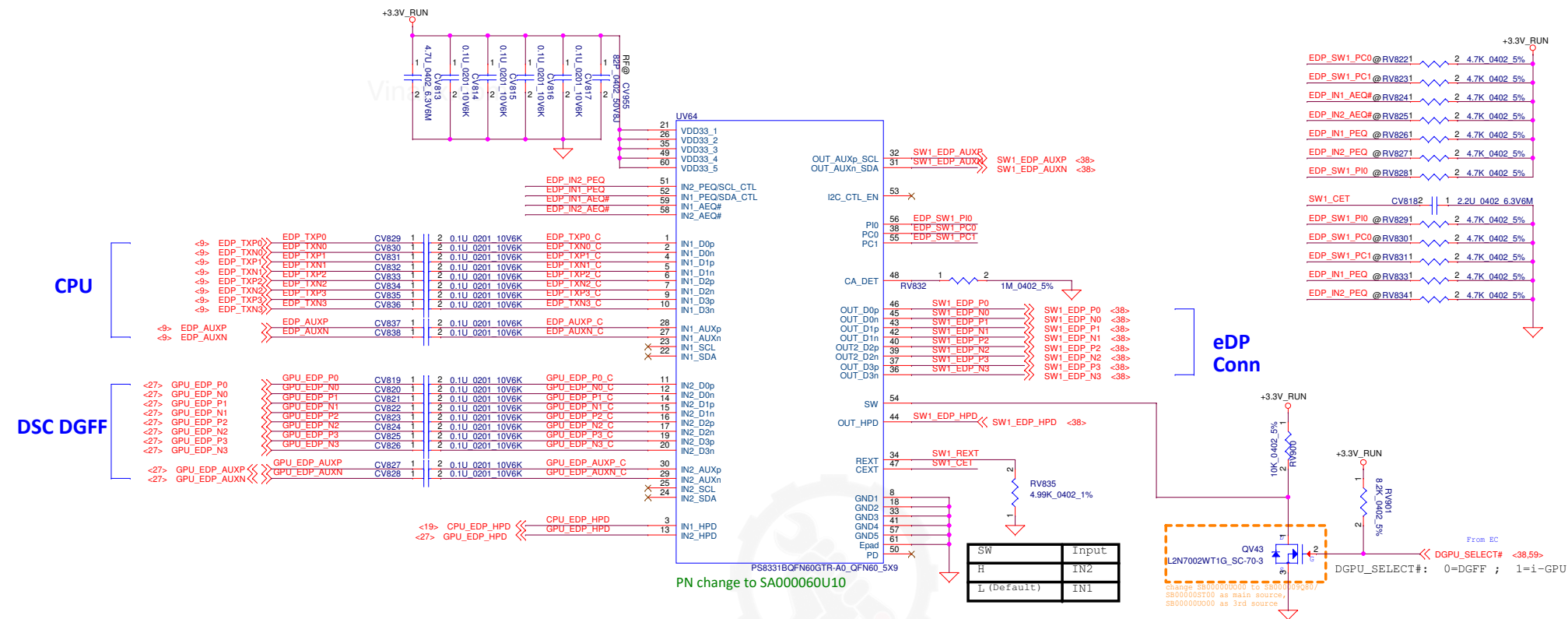
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UMA DGFF CON.



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2017/01/01		2017/01/01		Compal Electronics, Inc.	
2017/01/01		2017/01/01		LA-H281P	
2017/01/01		2017/01/01		Date: Tuesday, April 09, 2019	
2017/01/01		2017/01/01		Sheet 28 of 103	
2017/01/01		2017/01/01		Rev 1.0	

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INy_PEQ = Programmable input equalization levels
 L: default, LEQ, compensate channel loss up to 11.5dB @ HBR2
 H: HEQ, compensate channel loss up to 14.5dB @ HBR2
 M: LLEQ, compensate channel loss up to 8.5dB @ HBR2

INy_AEQ# = Automatic EQ disable
 L: Automatic EQ enable (default)
 H: Automatic EQ disable

PI0 = Auto test enable
 L: Auto test disable & input offset cancellation enable (default)
 H: Auto test enable & input offset cancellation enable
 M: Auto test disable & input offset cancellation disable

PC0 = AUX interception disable
 L: AUX interception enable, driver configuration is set by link training (default)
 H: AUX interception disable, driver output with fixed 800mV and 0dB
 M: AUX interception disable, driver output with fixed 400mV and 0dB

PC1 = Output swing adjustment
 L: default
 H: +20%
 M: -16.7%

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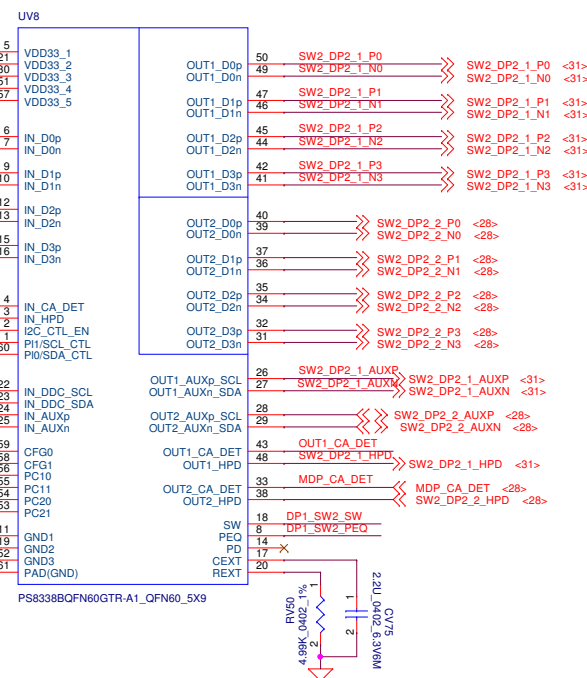
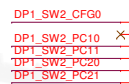
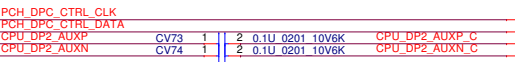
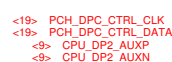
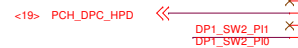
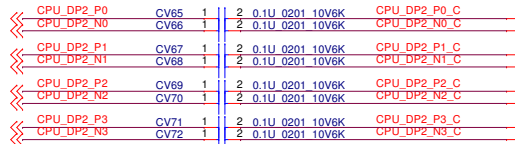
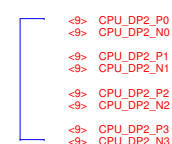
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eDP MUX (PS8331)

Security Classification	Compal Secret Data	
Issued Date	2016/01/01	Deciphered Date
		2017/01/01

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eDP MUX (PS8331)	LA-H281P	1.0
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TBT/MUX2

UMA DGFF

Port switching control or priority configuration. Internal pull down ~150KΩ, 3.3V I/O
For Control Switching Mode (CFG0 = L):
SW = L: Port1 is selected (default)
SW = H: Port2 is selected

For Automatic Switching Mode (CFG0 = H): (By OUT1_HPD and OUT2_HPD)
SW = L: Port1 has higher priority when both ports are plugged (default)
SW = H: Port2 has higher priority when both ports are plugged

	H	L
CFG0	V	
SW		V

Programmable input equalization levels. Internal pull down at ~150K Ω , 3.3V I/O
PEQ =

L: default, LEQ, compensate channel loss up to 11.5dB @ HBR2

H: HEQ, compensate channel loss up to 14.5dB @ HBR2

M: LLEQ, compensate channel loss up to 8.5dB @ HBR2

Overwritten by I2C register in I2C Control Mode

DSC DGFF

CPU

MUX1

TBT/DP

SW	DP1_GPU_SEL#
0	DGFF
1 (Default)	CPU

[IN_YEQ1/IN_YEQ0] =
LL: Compensate channel loss up to 8 dB @ HBR3
LM: Compensate channel loss up to 11 dB @ HBR3
LH: Compensate channel loss up to 14 dB @ HBR3
ML: Compensate channel loss up to 16 dB @ HBR3
MM: Compensate channel loss up to 17 dB @ HBR3
MH: Compensate channel loss up to 18 dB @ HBR3
HL: Compensate channel loss up to 19 dB @ HBR3
HM: Compensate channel loss up to 20 dB @ HBR3
HH: Compensate channel loss up to 21 dB @ HBR3

DSC DGFF

DEMUX

MUX2

TBT/DP

Reserve



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Size		DGPU					
Custom		Document Number					
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LA-H281P							

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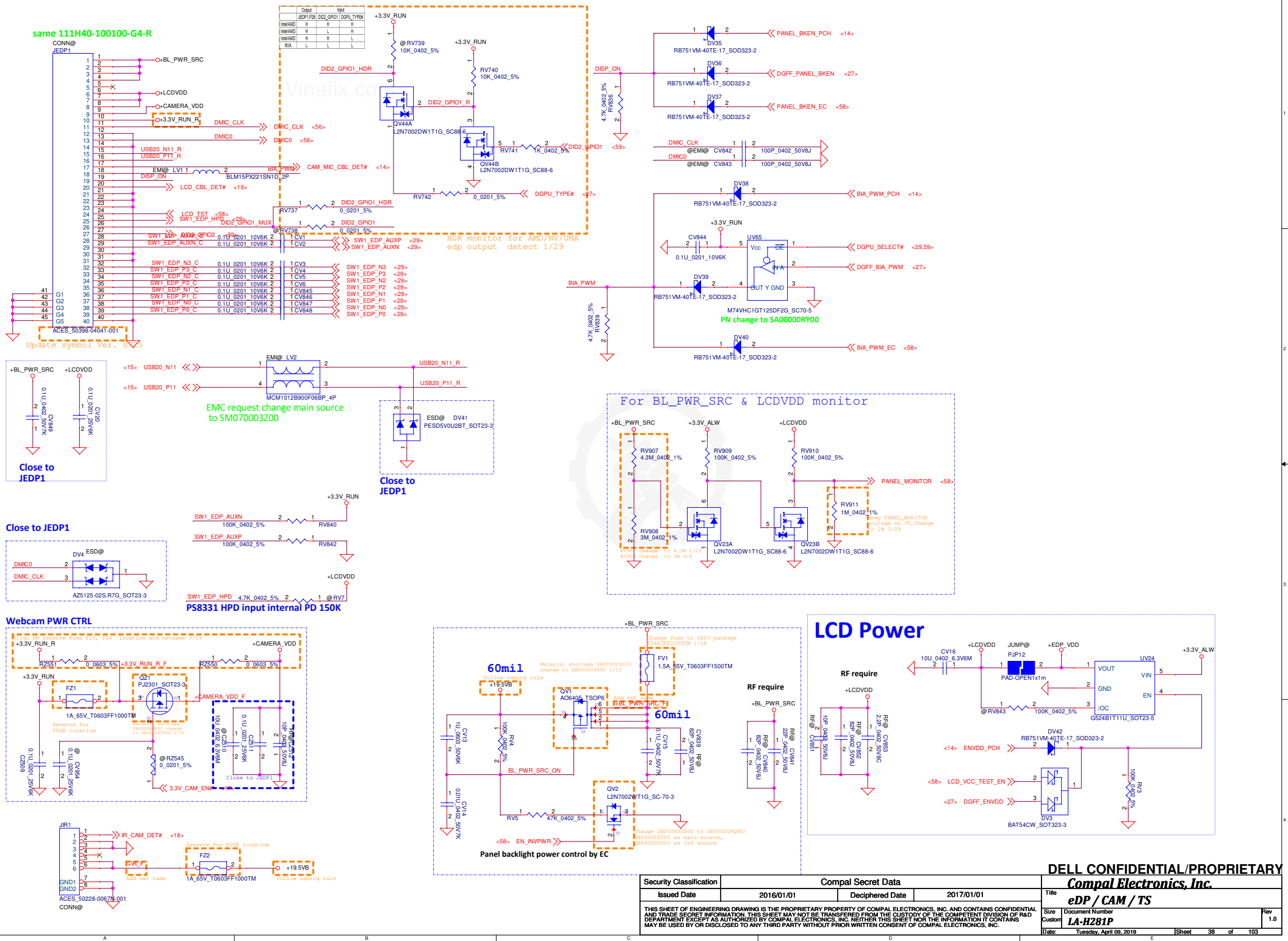
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Size	Custom	Rev	1.0
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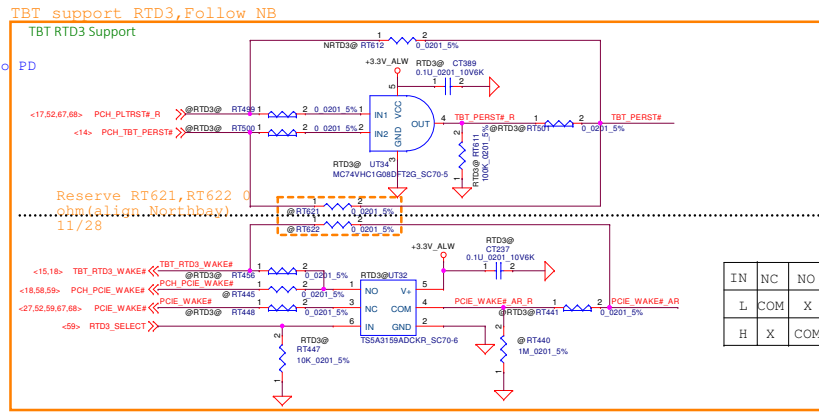
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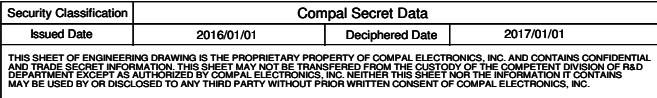
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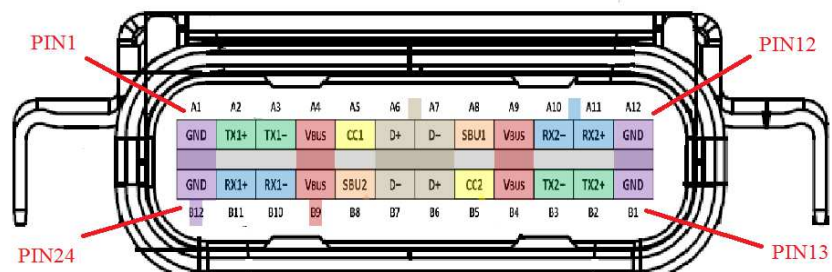
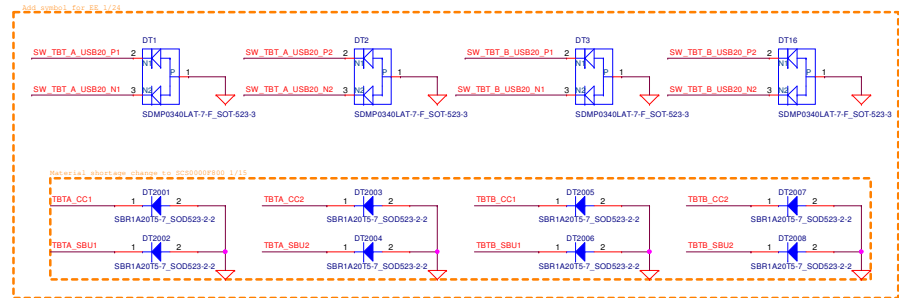
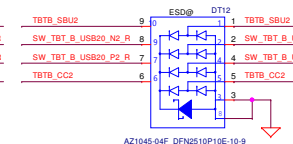
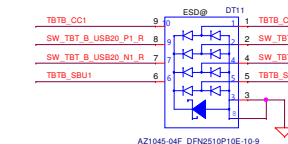
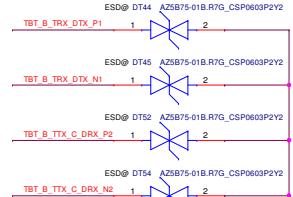
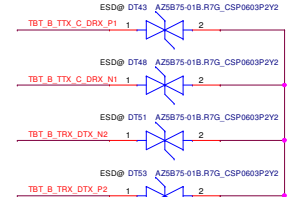
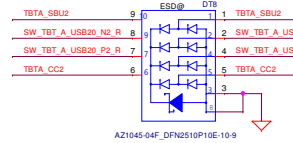
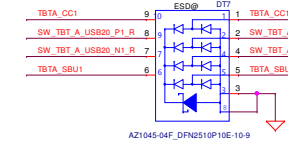
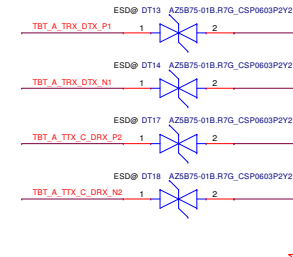
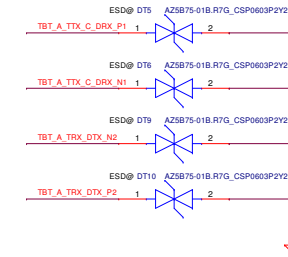
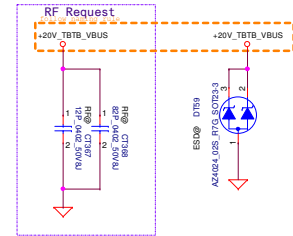
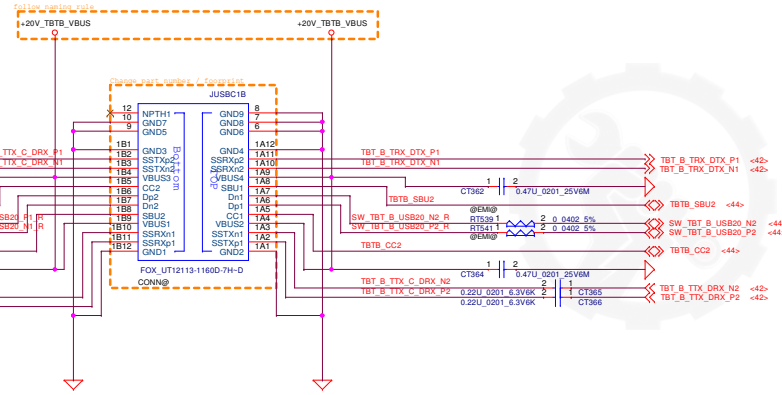
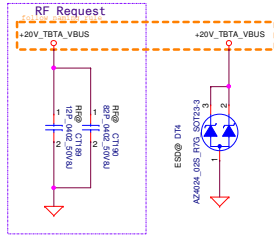
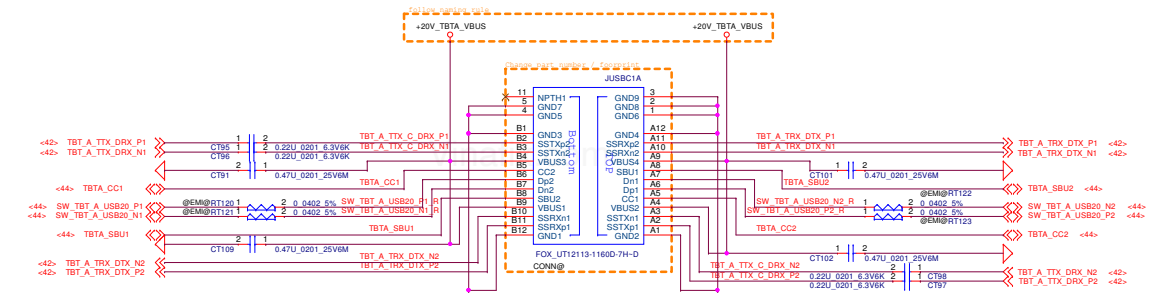
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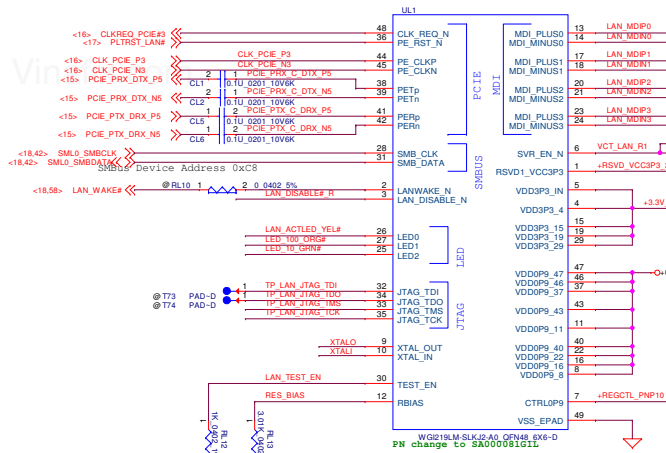
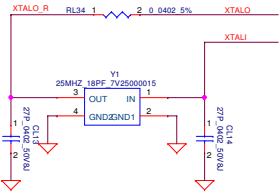
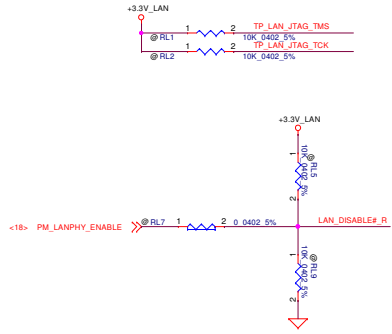
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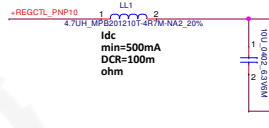
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				Size	Rev
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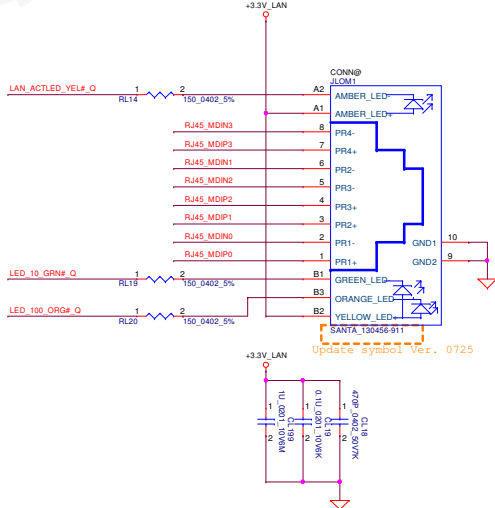
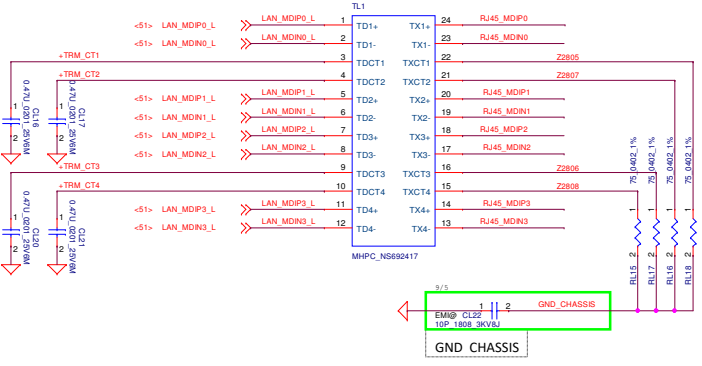


Note: +1.0V_LAN will work at 0.95V to 1.15V



Place C462, C463 and L29 close to U31

+3.3V_LAN/+3.3V_LAN_LOM:20mils

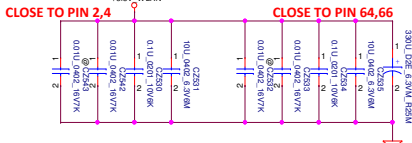
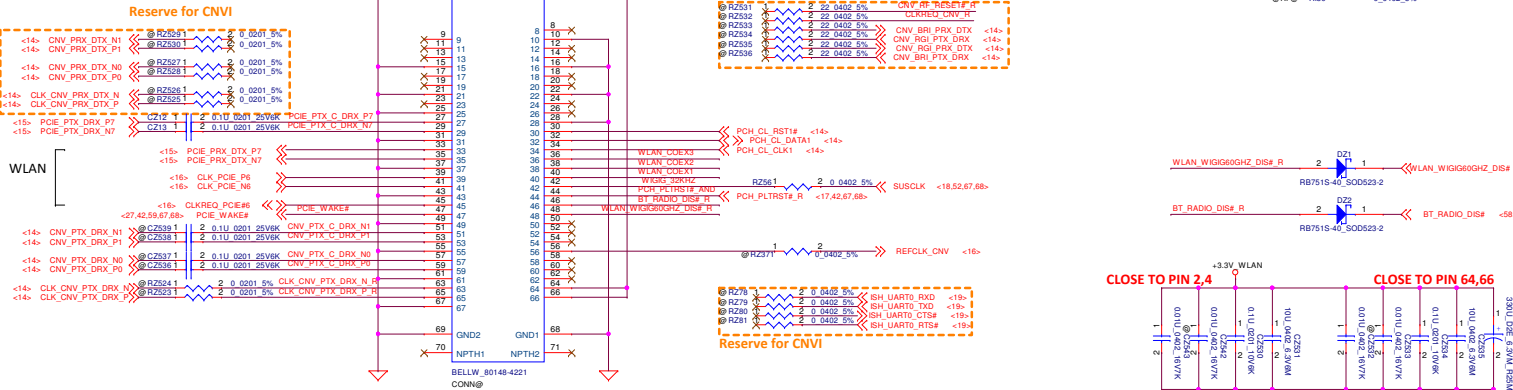


Close to J10M1

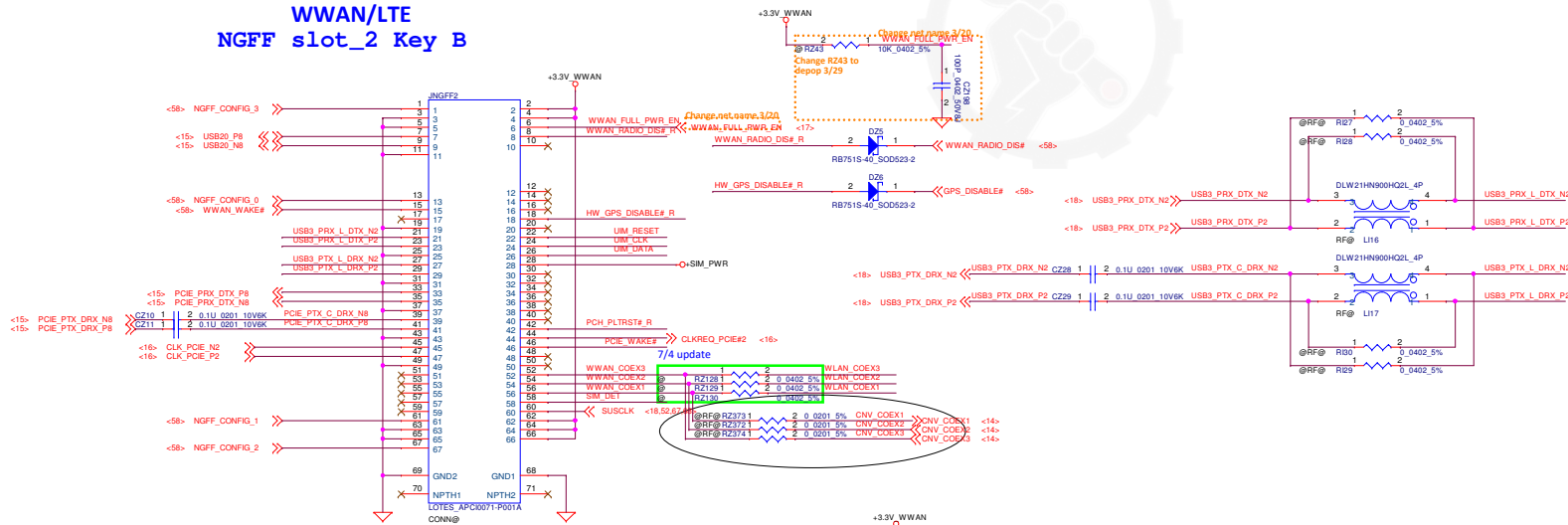
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LAN / LAN SW

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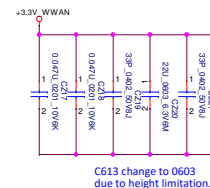
WLAN/BT
NGFF slot_1 Key A

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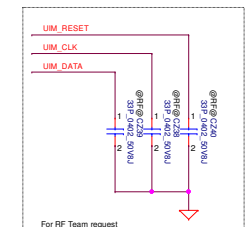
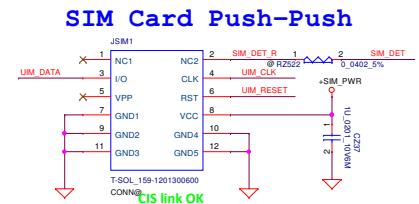
WWAN/LTE
NGFF slot_2 Key B



STATE #	CONFIG_0	CONFIG_1	CONFIG_2	CONFIG_3	Module Type
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8	1	0	0	0	WWAN
14	1	0	1	1	HCA-PCIE
15	1	1	1	1	Cache



C615 footprint change to C_APXK2R5ARA331MF451



DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.

WLAN (w/ CNVi) / WWAN

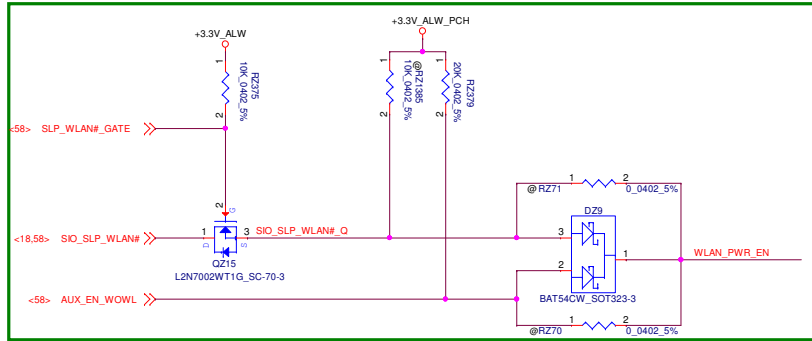
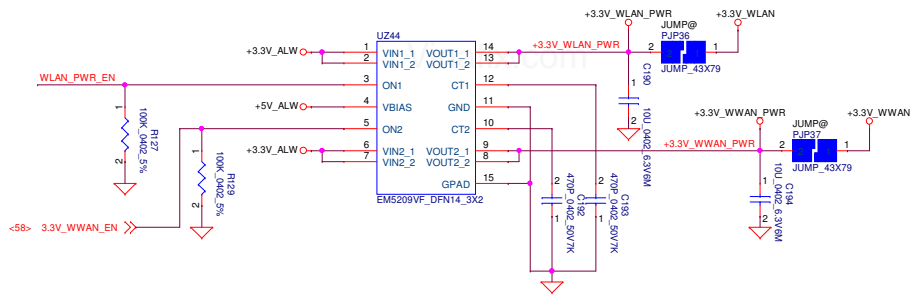
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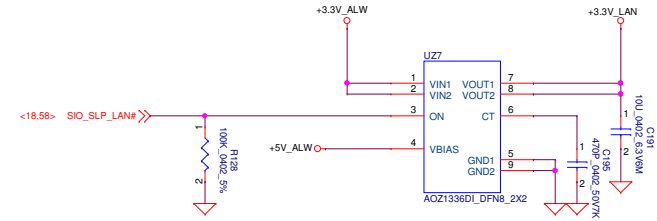
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Date:		Tuesday, April 09, 2019		Sheet 53 of 103	

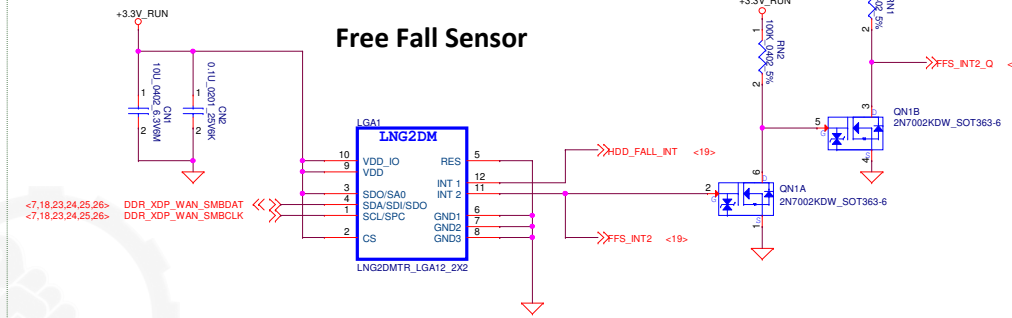
Power Control for WLAN & WWAN



Power Control for LAN

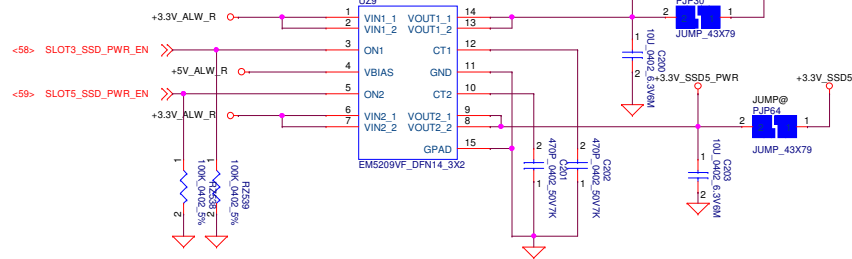


Free Fall Sensor

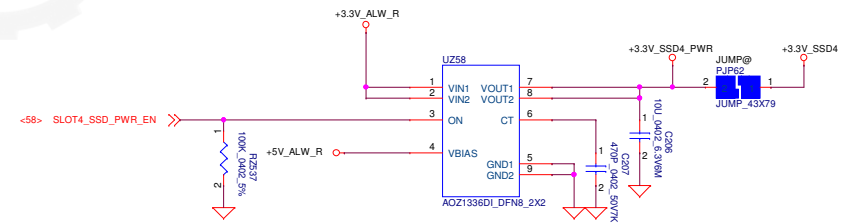


Power Control for M.2 slot 3. Source

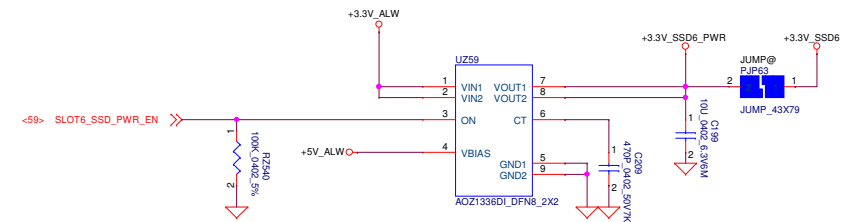
Power Control for M.2 slot 5. Source



Power Control for M.2 slot 4. Source



Power Control for M.2 slot 6. Source

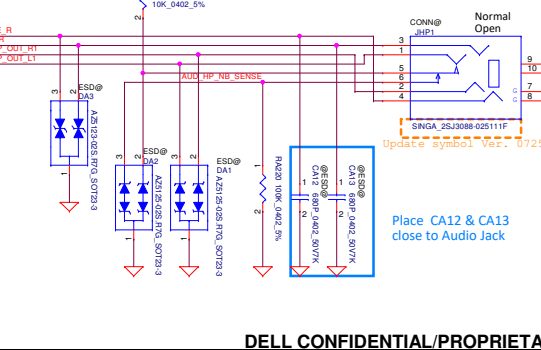
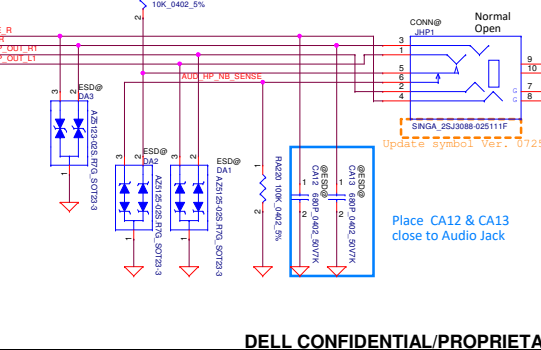
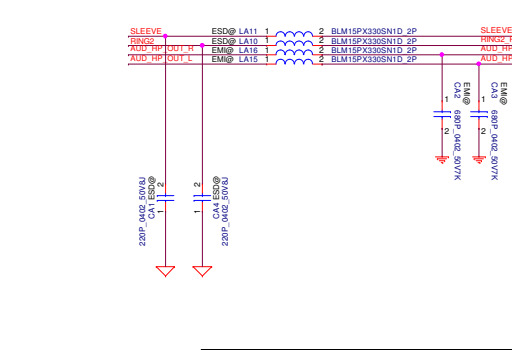
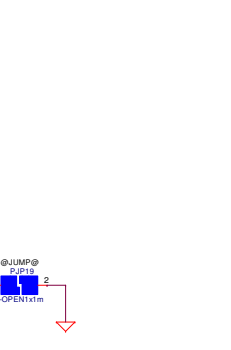


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					WLAN (w/ CNVi) / WWAN	
					Document Number	
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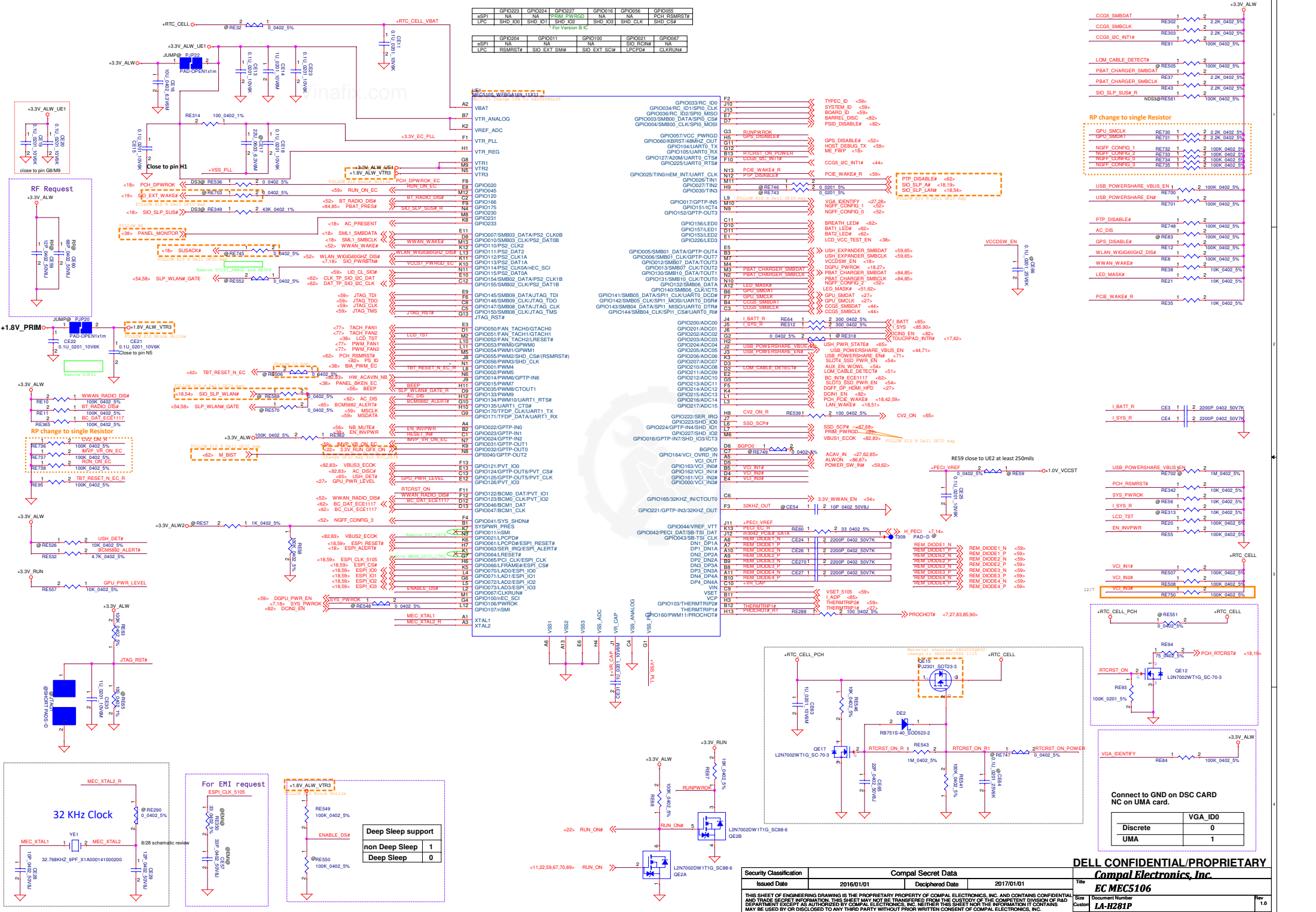
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				Version	1.0
				Created	06/01/2016
				Checked	06/01/2016

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				Document Number	
				LA-H281P	
				Rev 1.0	
Date: Tuesday, April 09, 2019				Sheet 57 of 103	



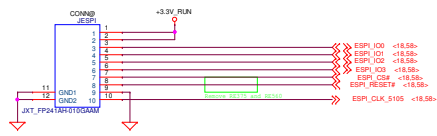
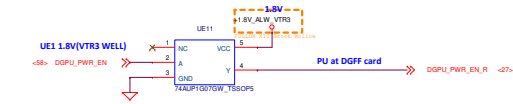
Connect to GND on DSC CARD
NC on UMA card.

Discrete	UMA
0	1

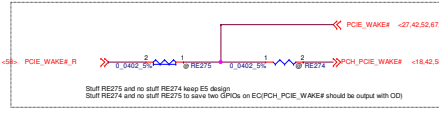
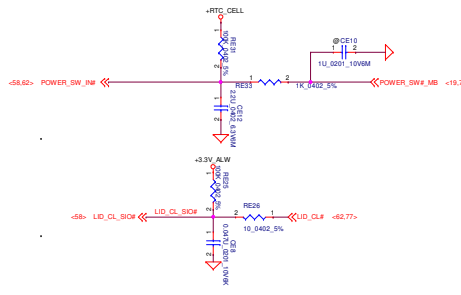
Security Classification
2016/01/01
Deciphered Date
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2017/01/01

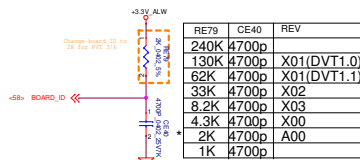


LPC 80Port Debug	LPC	ESPI
1	+3.3V_RUN	+3.3V_RUN
2	+3.3V_RUN	+3.3V_RUN
3	LPC_LAD0	ESPI_I00
4	LPC_LAD1	ESPI_I01
5	LPC_LAD2	ESPI_I02
6	LPC_LAD3	ESPI_I03
7	LPC_FRAME	ESPI_CS#
8	PCH_PLTRST#	NA
9	GND	GND
10	LPC_CLOCK	ESPI_CLK

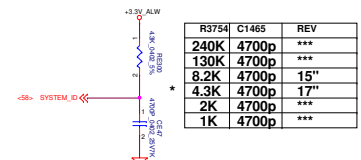


RE343	CE62	REV
240K	4700p	Single Port ACE w/o AR
130K	4700p	Single Port ACE w/AR
62K	4700p	Dual Port ACE w/o AR
33K	4700p	Dual Port ACE w/AR
8.2K	4700p	Dual Port ACE (w/AR + w/o AR)
4.3K	4700p	-
2K	4700p	-
1K	4700p	-

TypeC_ID rise time is measured from 5%-68%

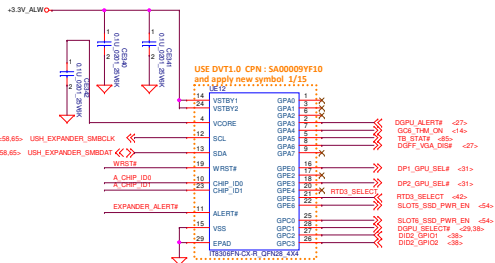


BOARD_ID rise time is measured from 5%-68%



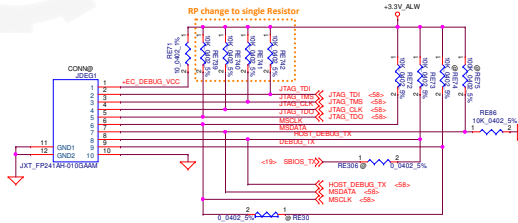
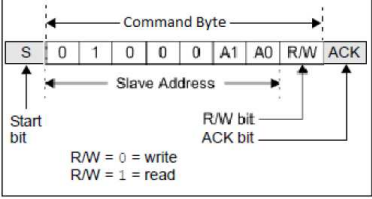
PANEL_ID rise time is measured from 5%-68%

SIO IT8306



For I2C SAD+Read/Write patterns

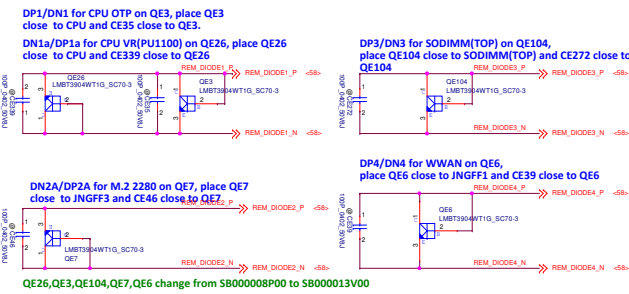
Command	SAD[7:3]	ID[1]	ID[0]	R/W	SAD+R/W
Read	01000	0	0	1	01000001 (41h)
Write	01000	0	0	0	01000000 (40h)
Read	01000	0	1	1	01000011 (43h)
Write	01000	0	1	0	01000010 (42h)
Read	01000	1	0	1	01000101 (45h)
Write	01000	1	0	0	01000100 (44h)
Read	01000	1	1	1	01000111 (47h)
Write	01000	1	1	0	01000110 (46h)



Rest=1.58k, Tp=96 degree



Channel	Location
DP1/DN1	CPU OTP
DP1A/DN1A	CPU VR
DP2A/DN2A	M.2 2280
DP3/DN3	DIMM(TOP)
DP4/DN4	WWAN



QE26, QE3, QE104, QE7, QE6 change from S8000008P00 to S8000013V00

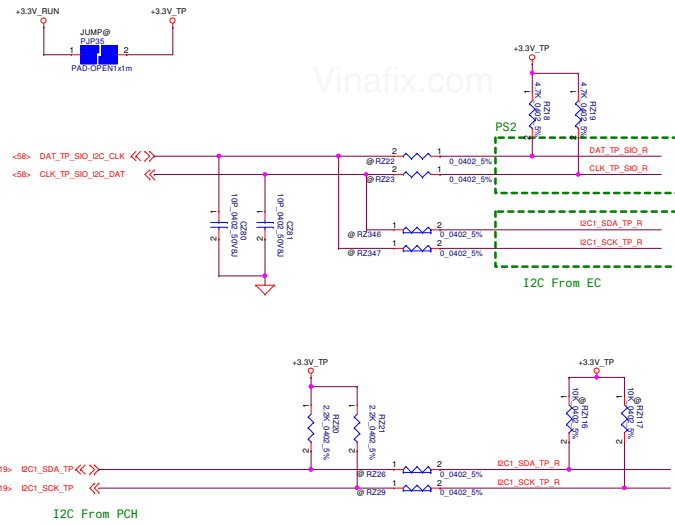
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1		103		1.0	

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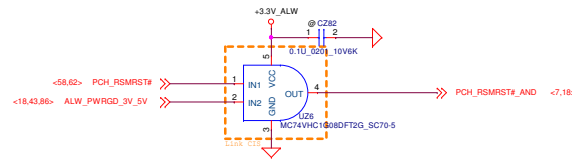
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Touch Pad

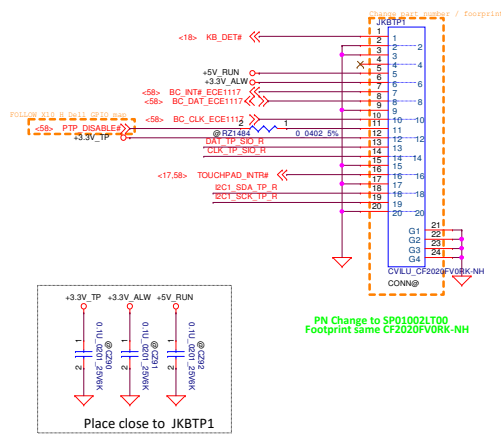


Plan is for I2C to be driven by the EC for Win7 and Pre-OS (will utilize Intel I2C drivers for Win7). For Win8.1 and 10 the EC will control TP over I2C Pre-OS and then the PCH will drive I2C when in Windows. Route PS2 from EC to the touch pad also for contingency plan if I2C has issues.

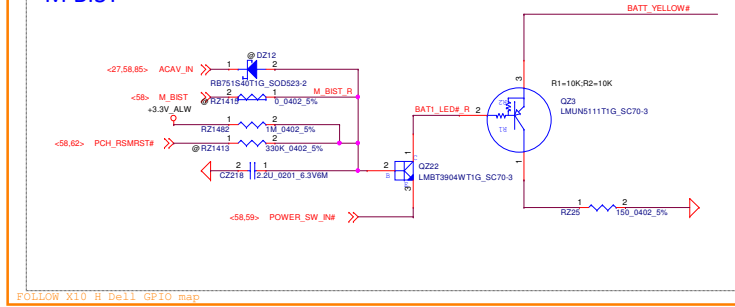
RSMRST circuit



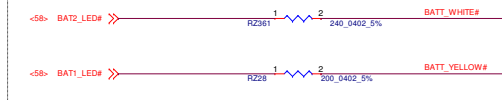
Keyboard



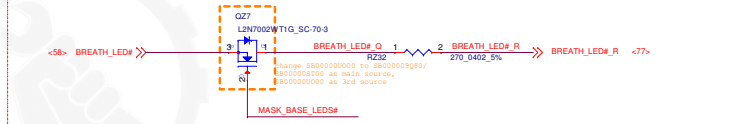
M BIST



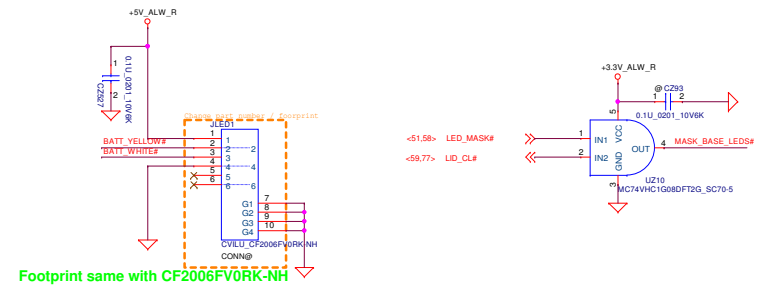
Battery LED



Breath LED



To LED/B Conn



LED Circuit Control Table

	LED_MASK#	LID_CL#
Mask All LEDs (Sniffer Function)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1

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KB / LED / LID

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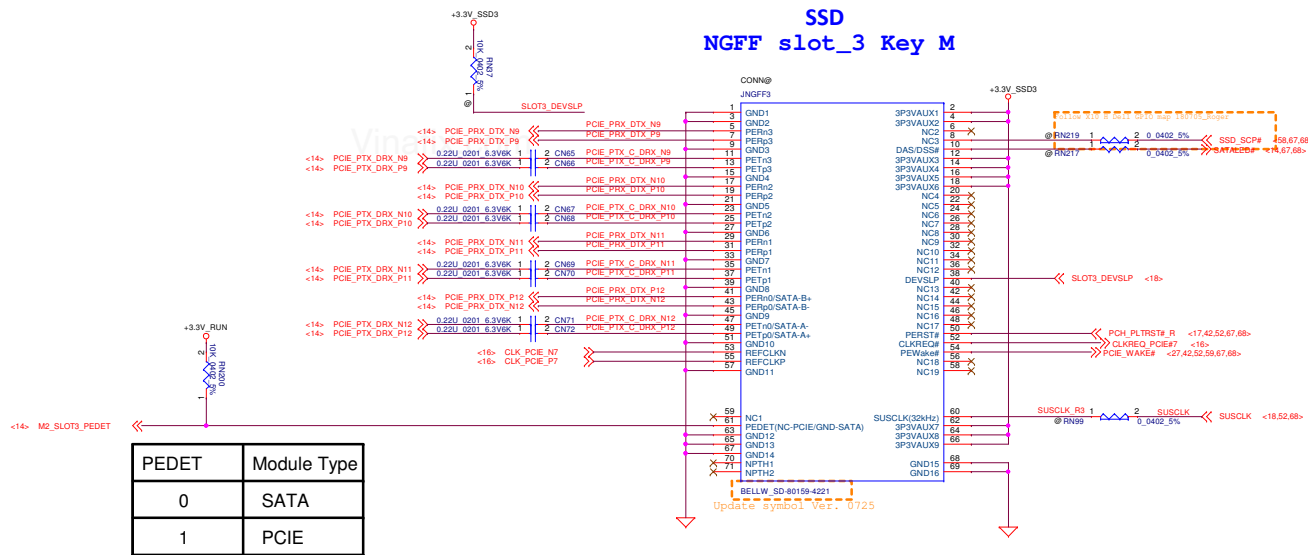
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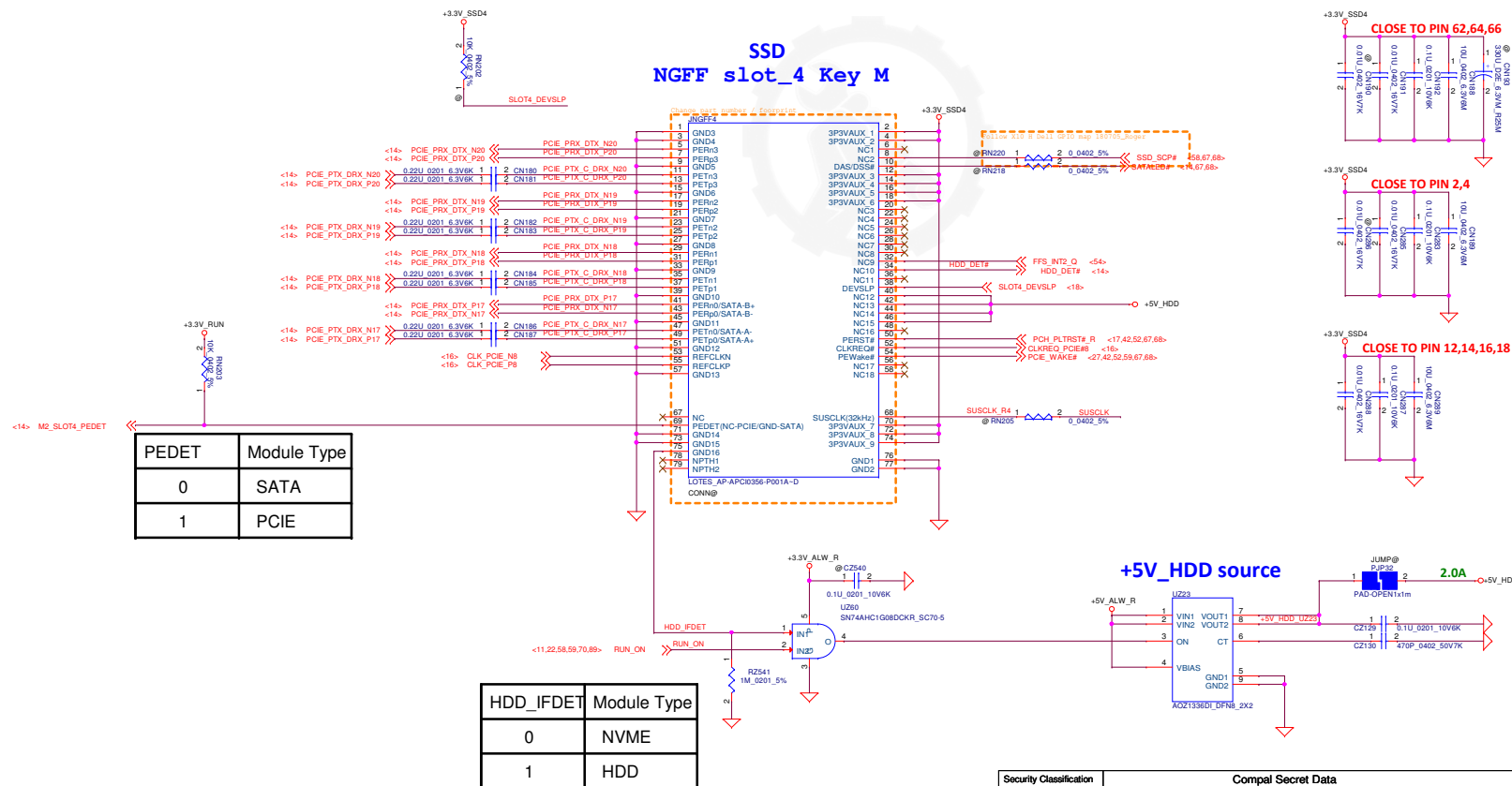
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SSD NGFF slot_3 Key M

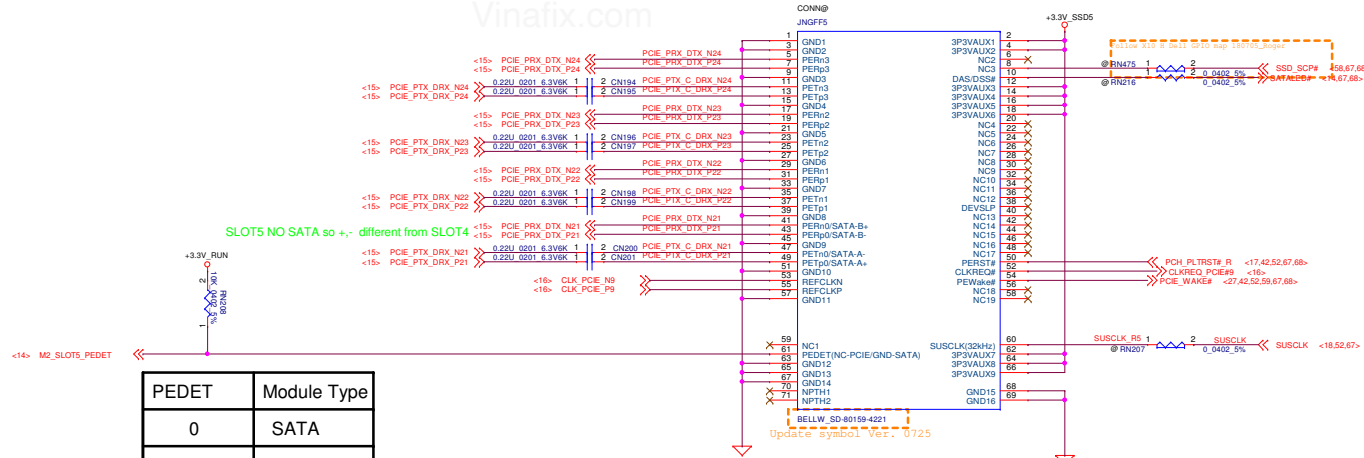


SSD NGFF slot_4 Key M

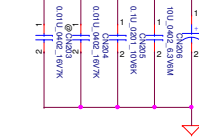


SSD NGFF slot_5 Key M

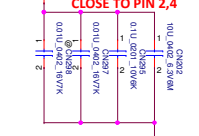
Vinafix.com



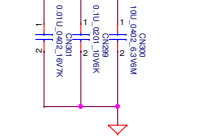
CLOSE TO PIN 62,64,66



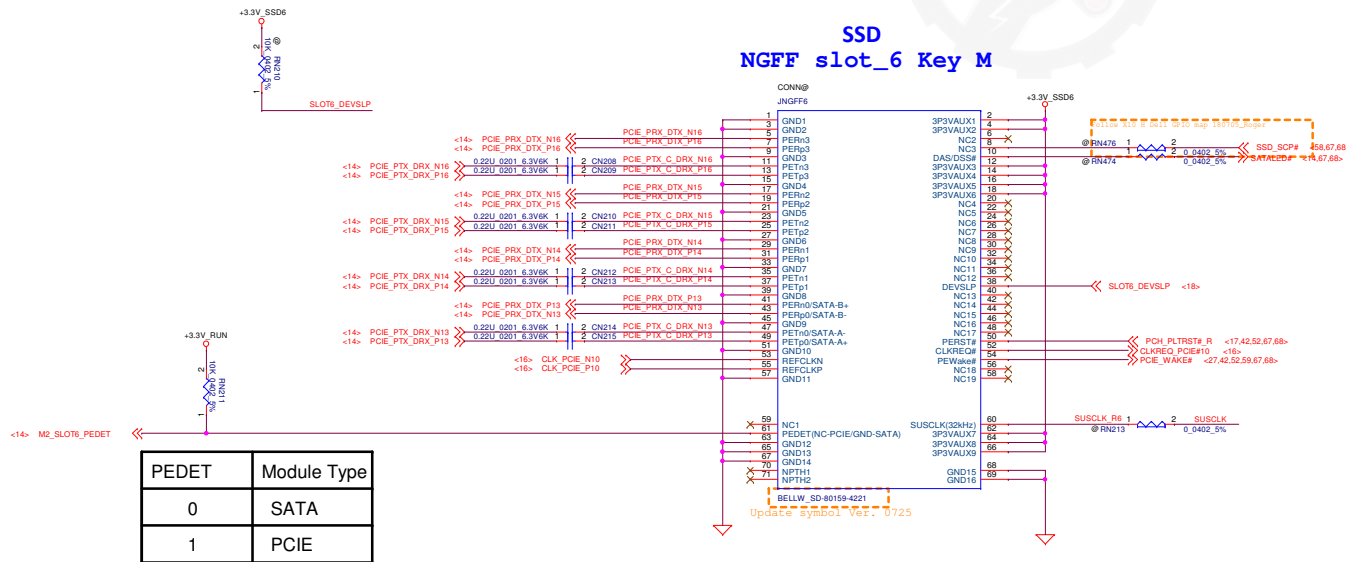
CLOSE TO PIN 2,4



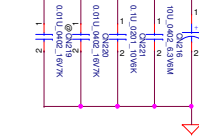
CLOSE TO PIN 12,14,16,18



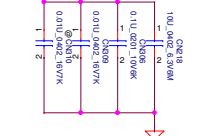
SSD NGFF slot_6 Key M



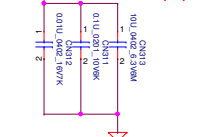
CLOSE TO PIN 62,64,66



CLOSE TO PIN 2,4



CLOSE TO PIN 12,14,16,18



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SSD SLOTS / 6

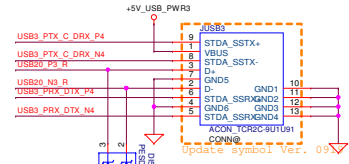
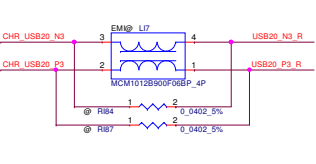
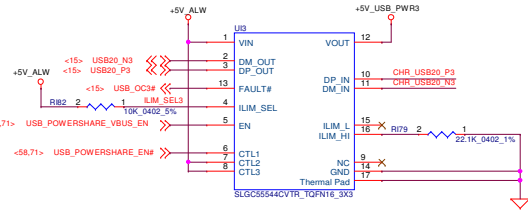
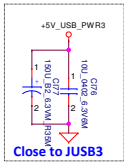
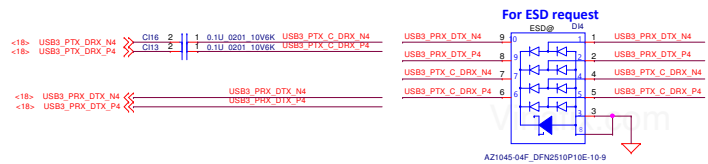
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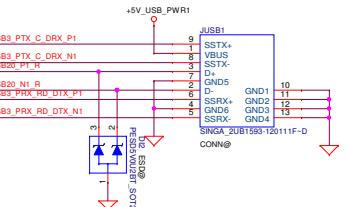
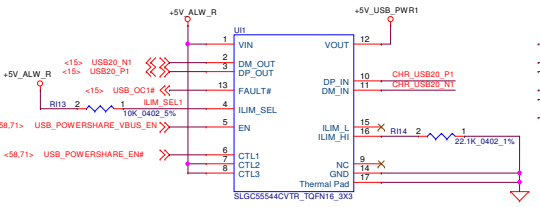
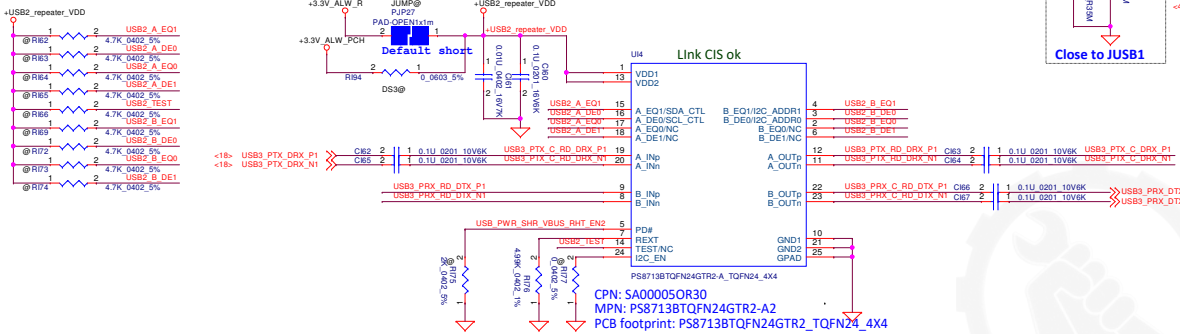
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Date:	Tuesday, April 05, 2018	Sheet 68 of 103

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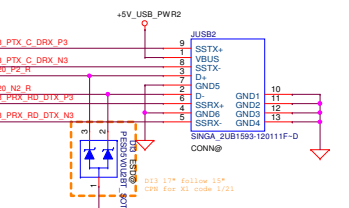
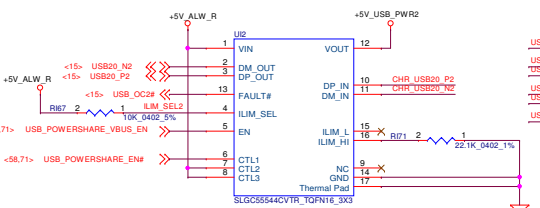
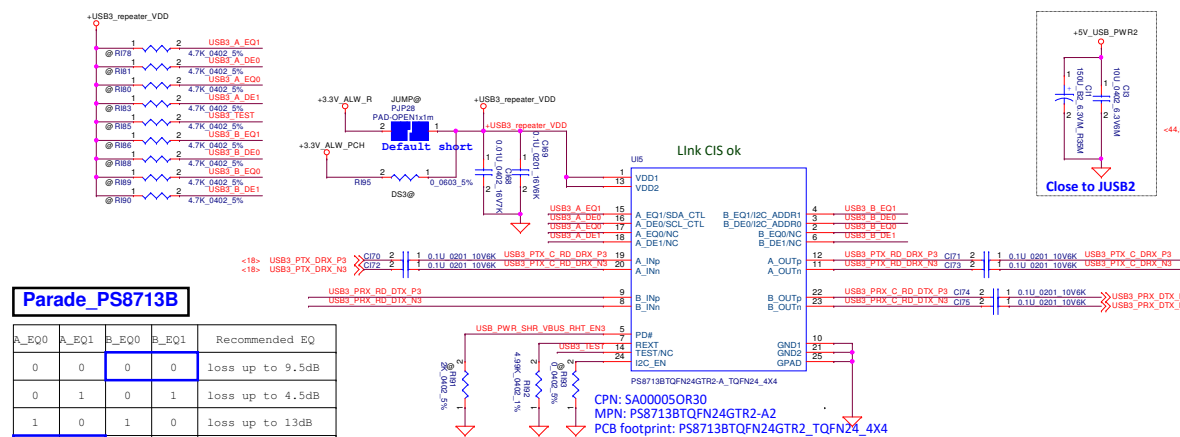
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JUSB3



JUSB1



JUSB2

Parade PS8713B

A_EQ0	A_EQ1	B_EQ0	B_EQ1	Recommended EQ
0	0	0	0	loss up to 9.5dB
0	1	0	1	loss up to 4.5dB
1	0	1	0	loss up to 13dB
1	1	1	1	loss up to 7.5dB

Both A_EQ&B_EQ have internal pull-down 150k

Reserve

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								USB2/USB3 TYPEA	
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						Custom	LA-H281P		1.0
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								USB2/USB3 DB					
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				Rev	1.0

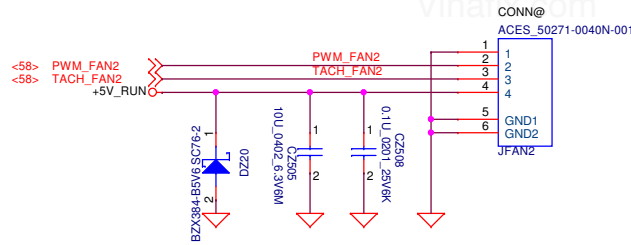
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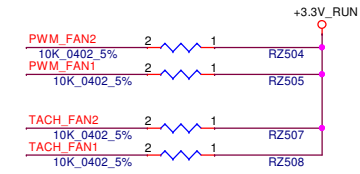
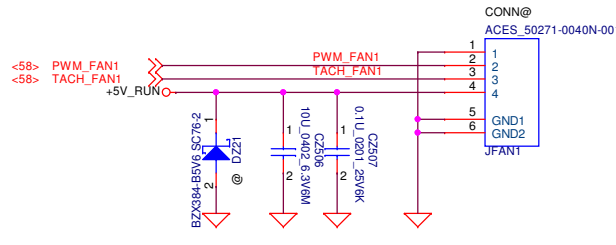
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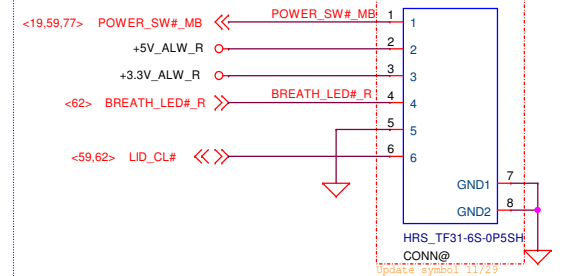
DGFF FAN



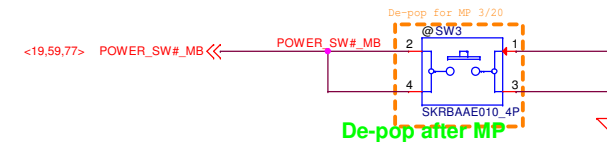
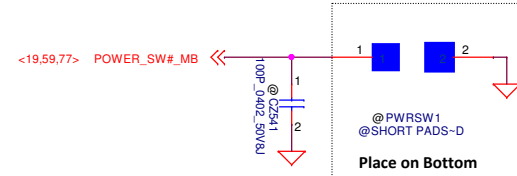
CPU FAN



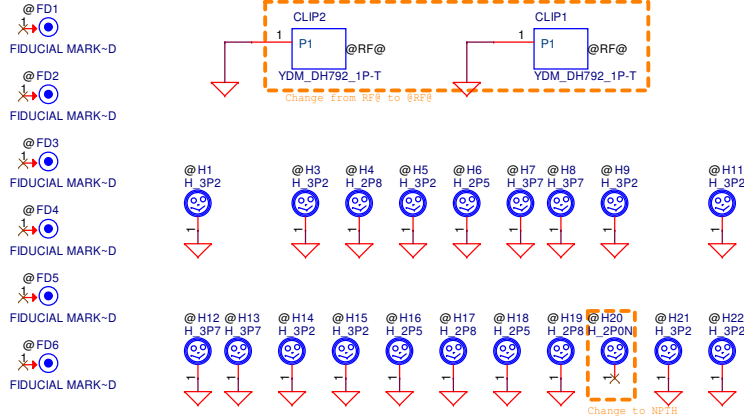
Power Button CONN



Power Switch for debug



Fiducial Mark



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				Compal Electronics, Inc.	
				PWRBTN / /SCREW / FAN	
				Size	Document Number
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Issued Date		2016/01/01		Deciphered Date		2017/01/01		Title		
								XDP/CMC/APS...debug		
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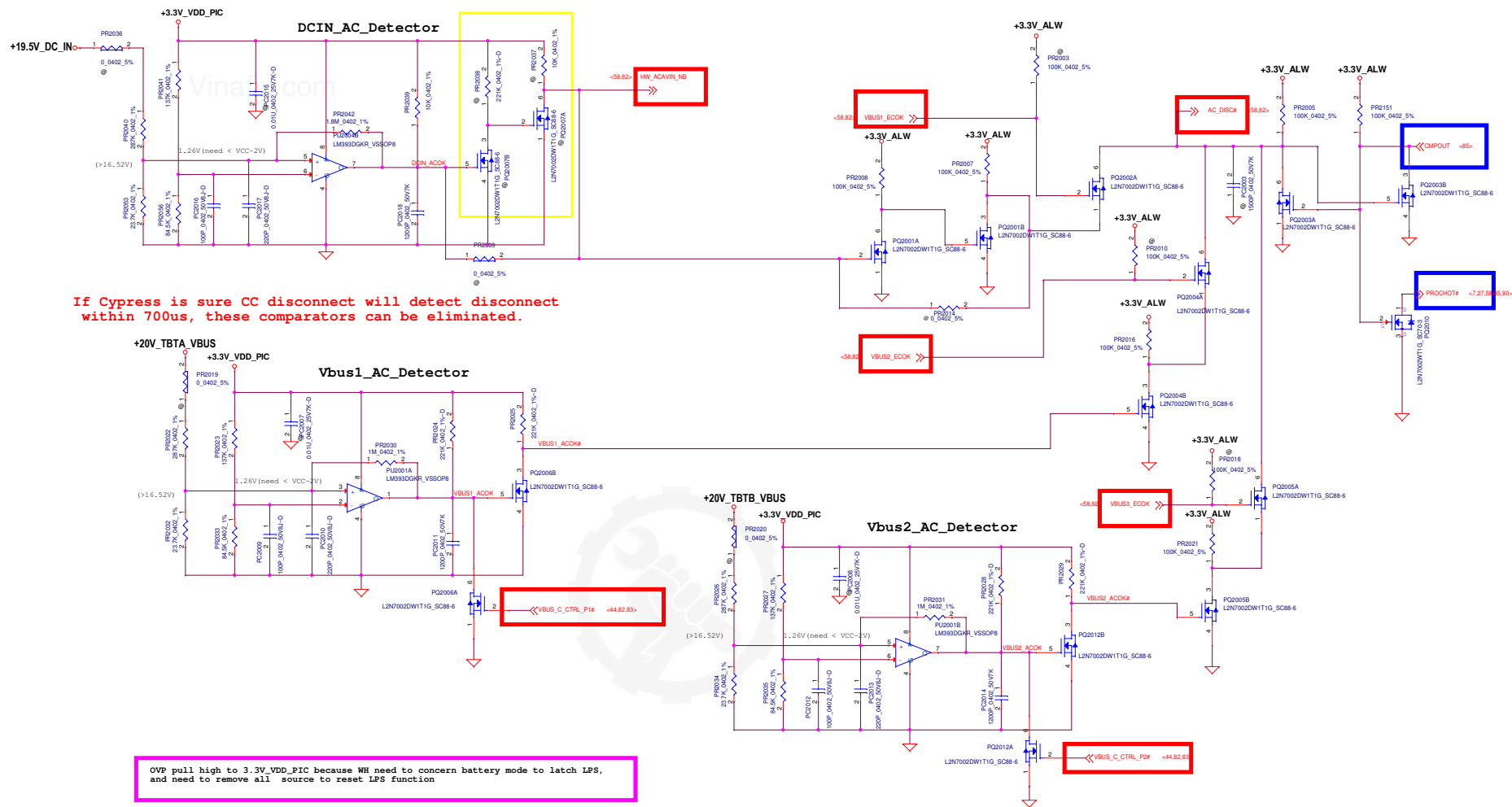
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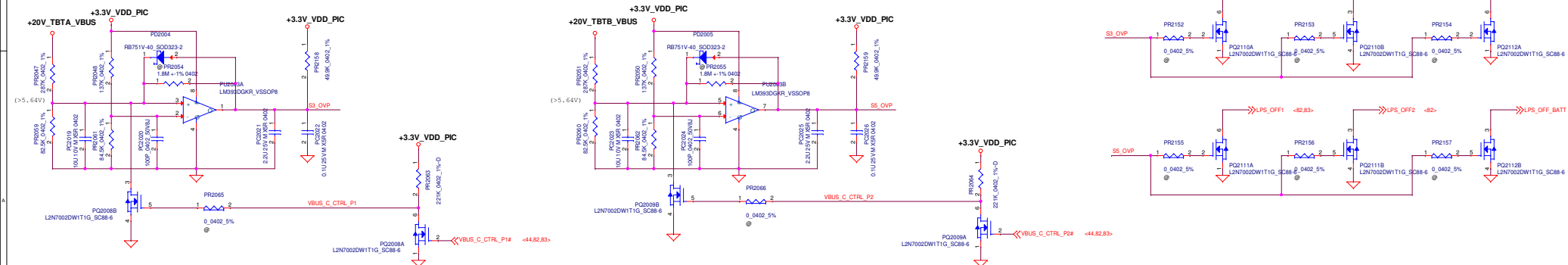


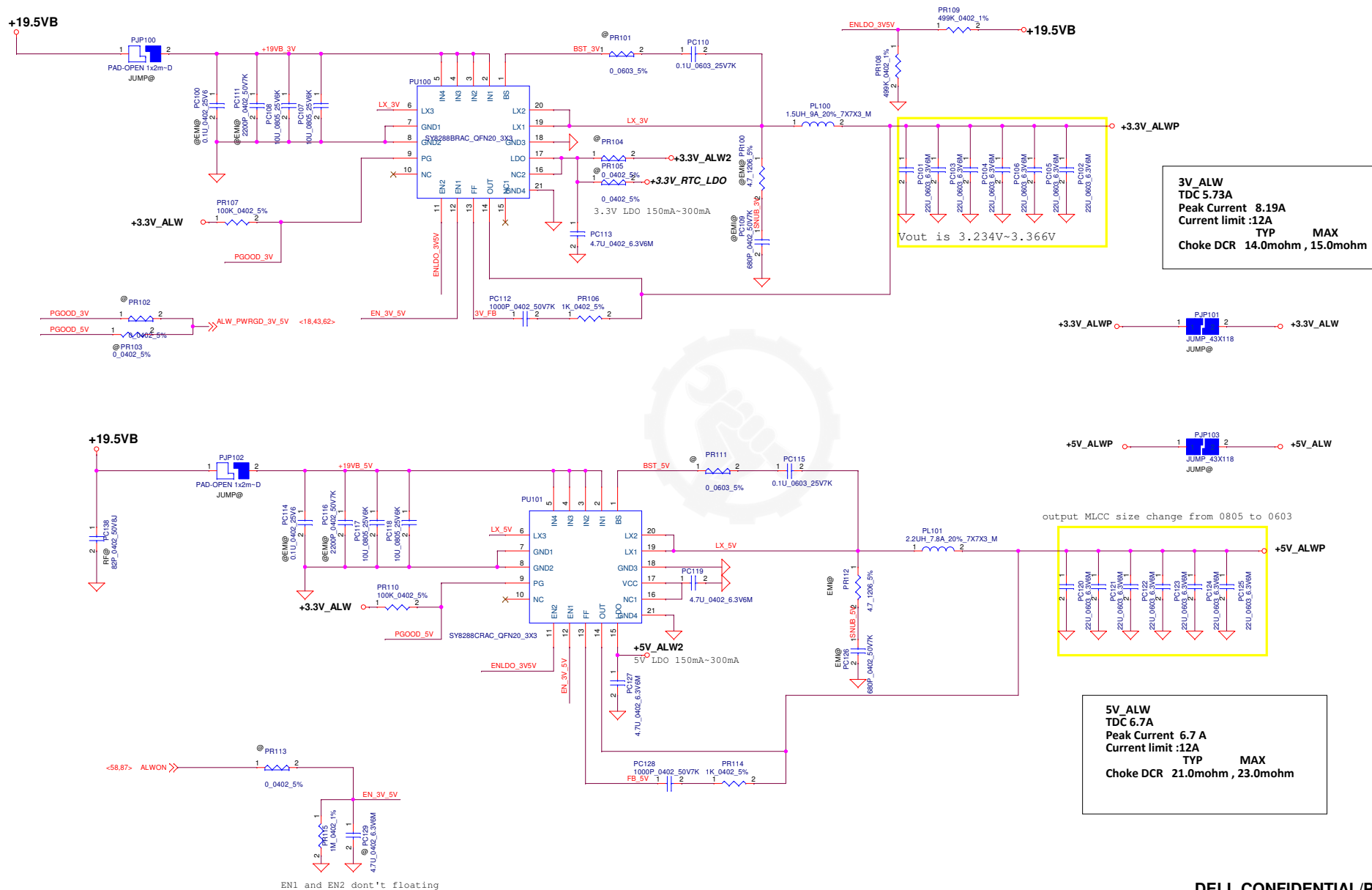
Compal Electronics, Inc.		
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Reserve		
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S3 OVP

S5 OVP





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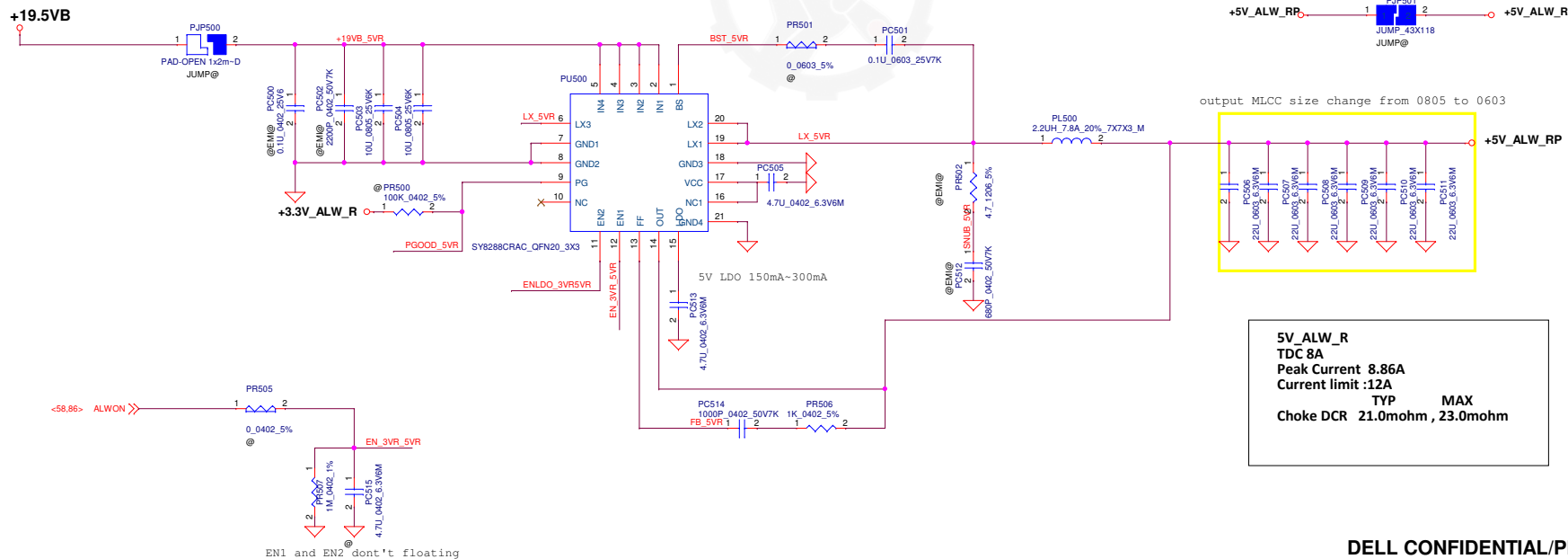
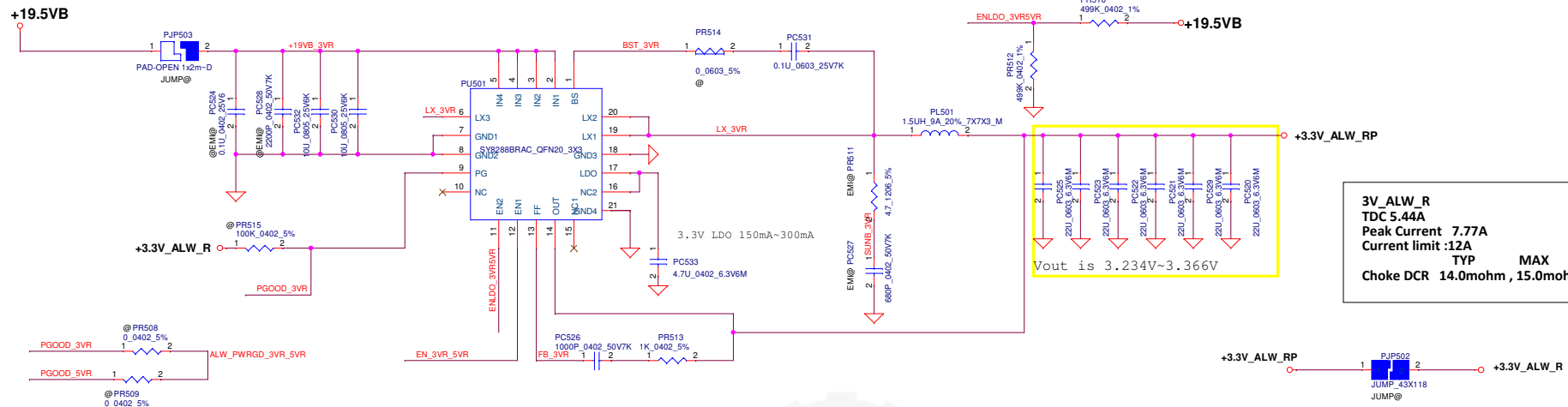


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5V ALW/3V ALW

LA-H281P

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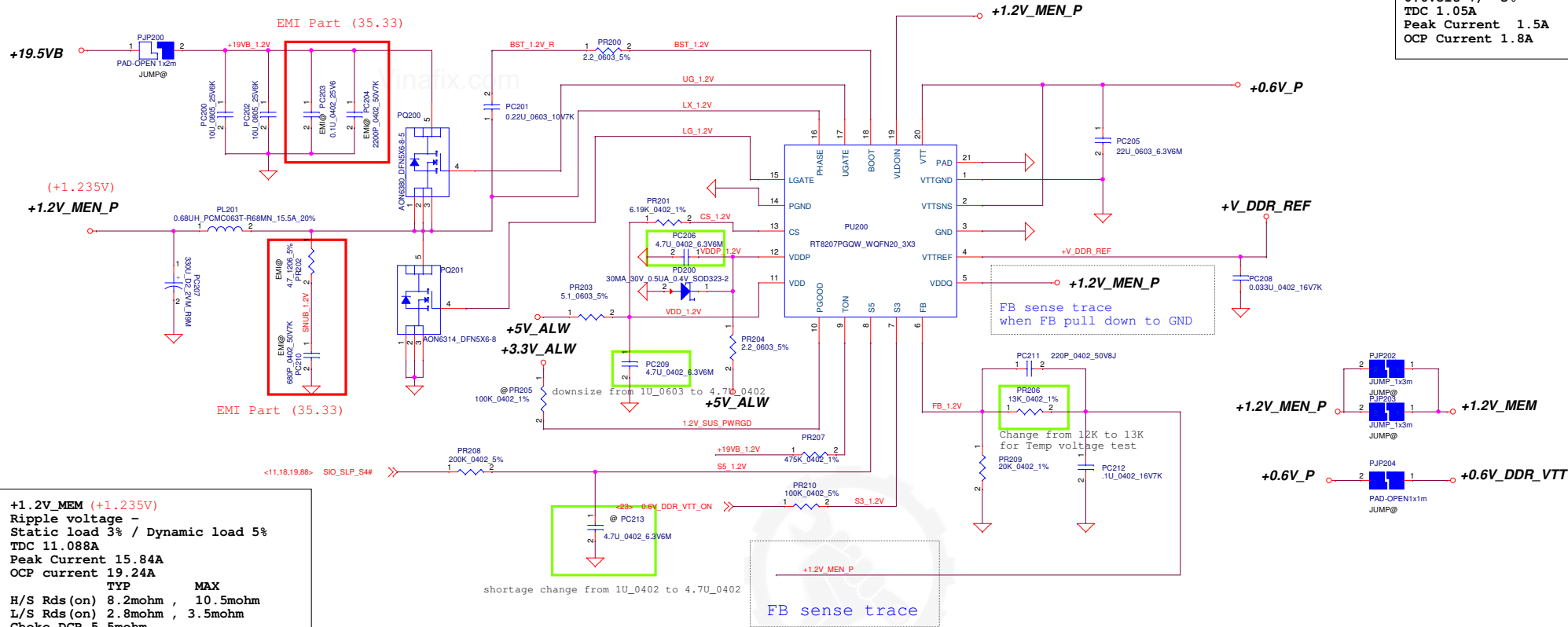
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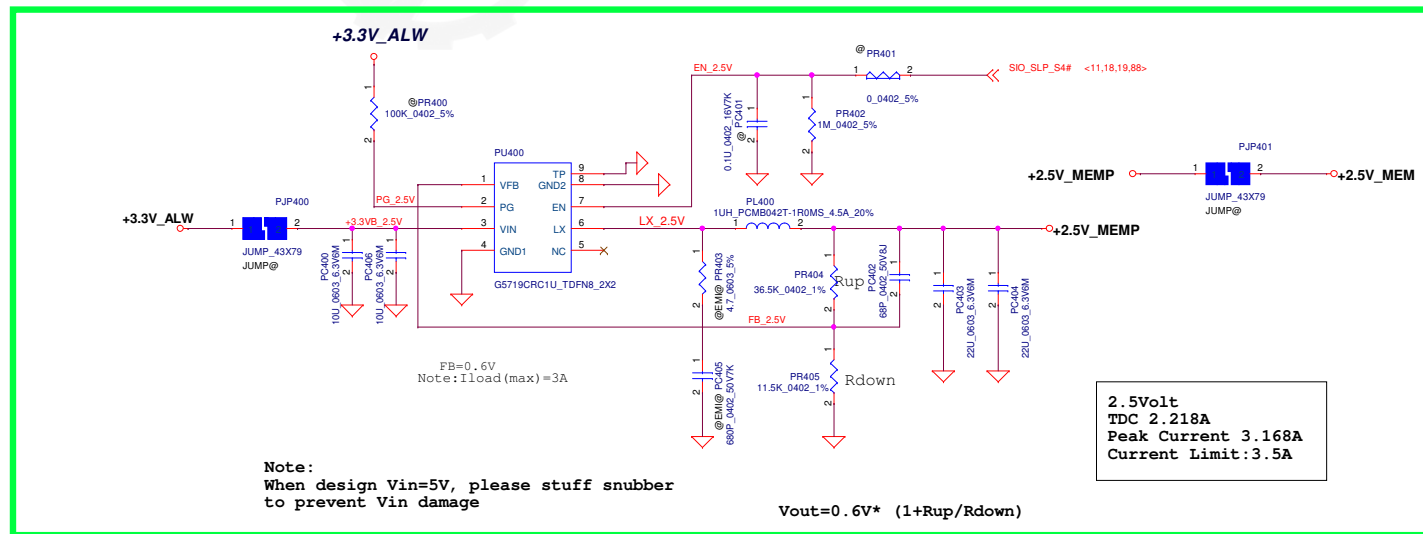


Compal Electronics, Inc.		
5V_ALW_R/3V_ALW_R		
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+1.2V_MEM (+1.235V)
 Ripple voltage -
 Static load 3% / Dynamic load 5%
 TDC 11.088A
 Peak Current 15.84A
 OCP current 19.24A
 TYP MAX
 H/S Rds(on) 8.2mohm , 10.5mohm
 L/S Rds(on) 2.8mohm , 3.5mohm
 Choke DCR 5.5mohm
 Bulk cap ESR 9mohm
 Switching Frequency: 533kHz

Mode	S3	S5	+1.2V_MEN_P	+V_DDR_REF	+0.6V_P
S5	L	L	off	off	off
S3	L	H	on	on	off (Hi-Z)
S0	H	H	on	on	on



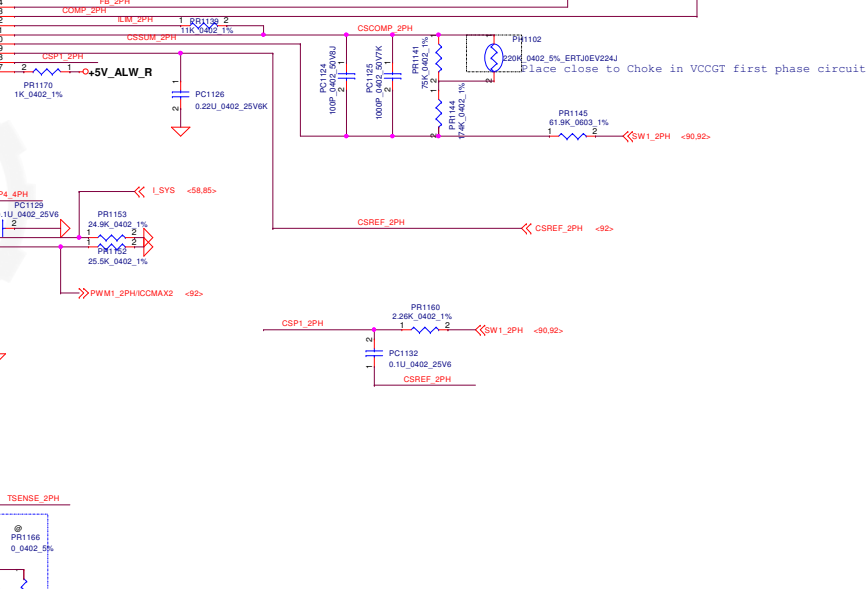
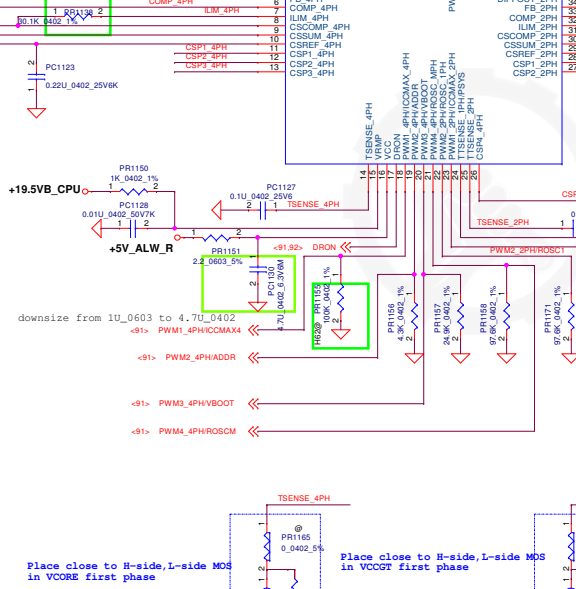
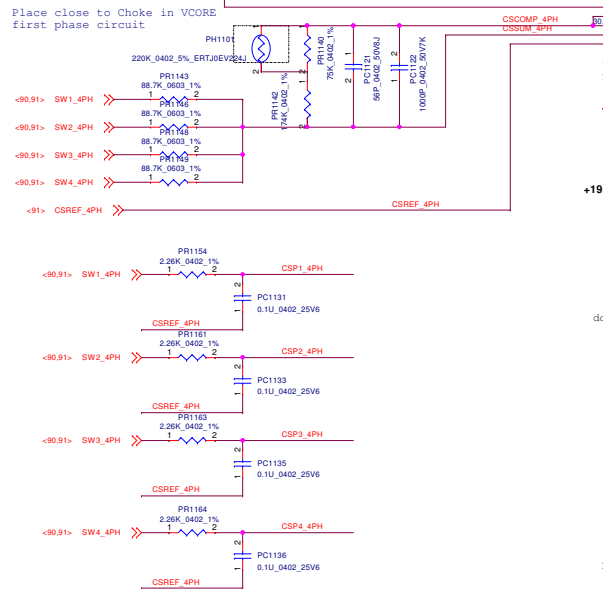
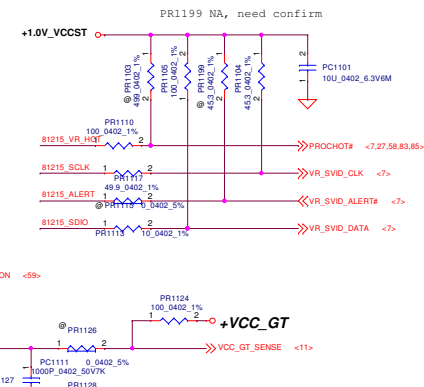
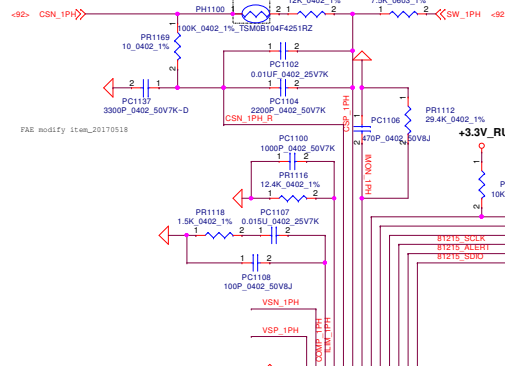
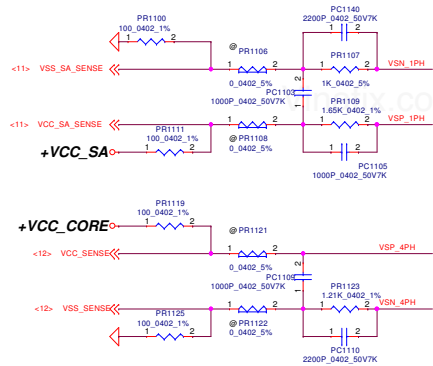
2.5Volt
 TDC 2.218A
 Peak Current 3.168A
 Current Limit: 3.5A


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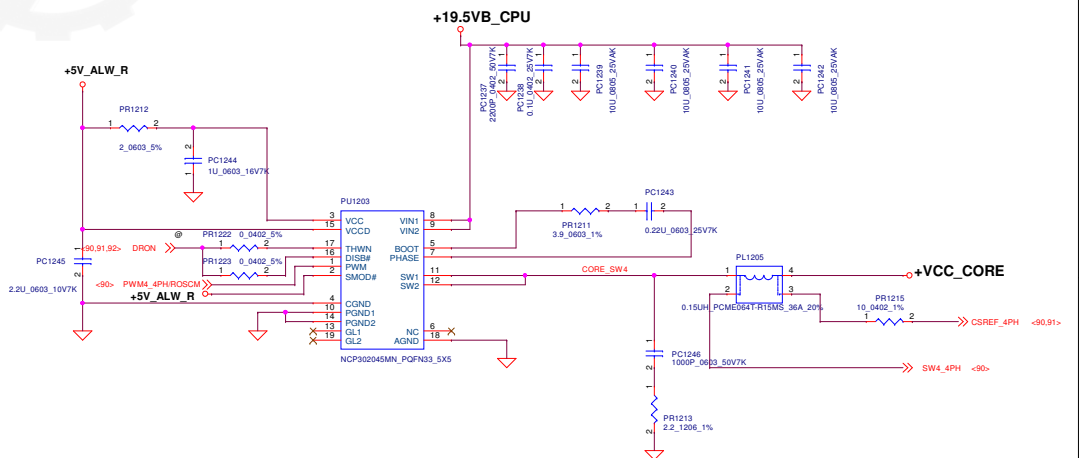
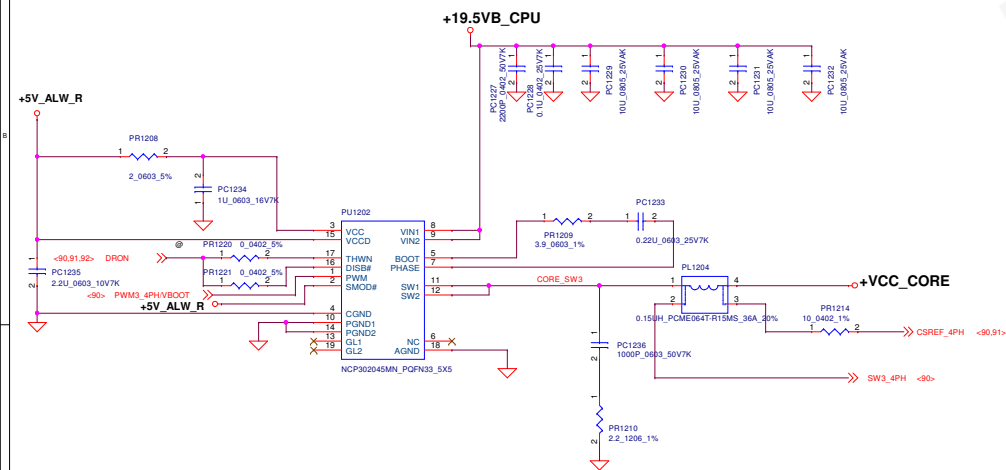
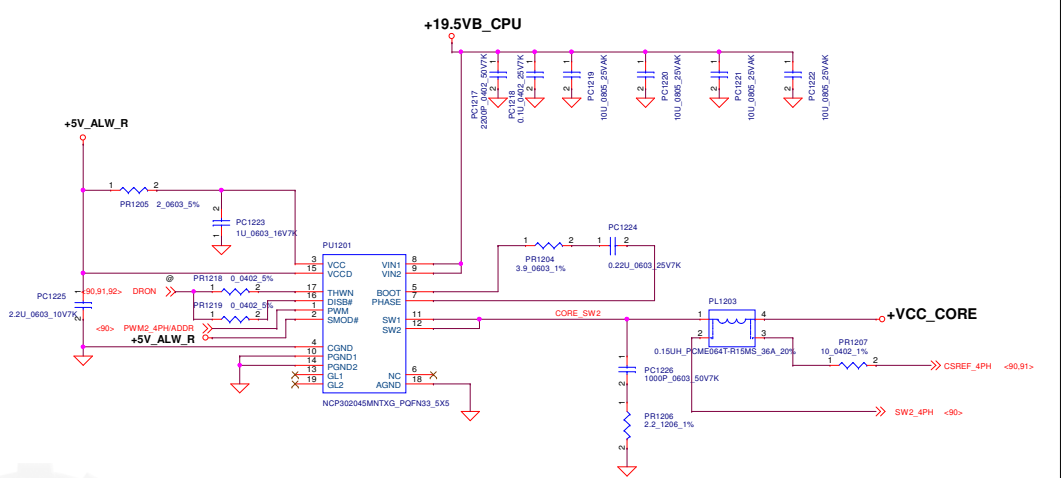
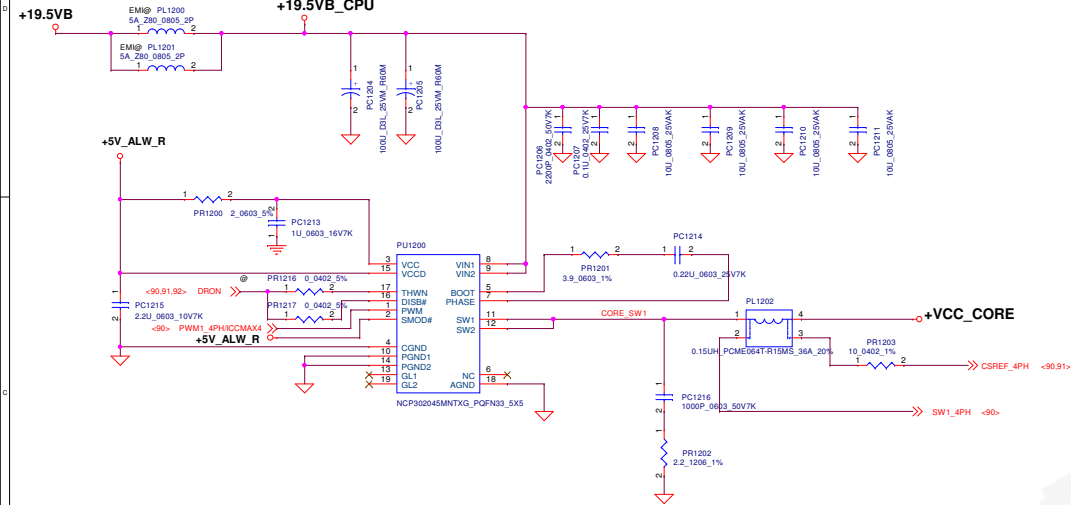
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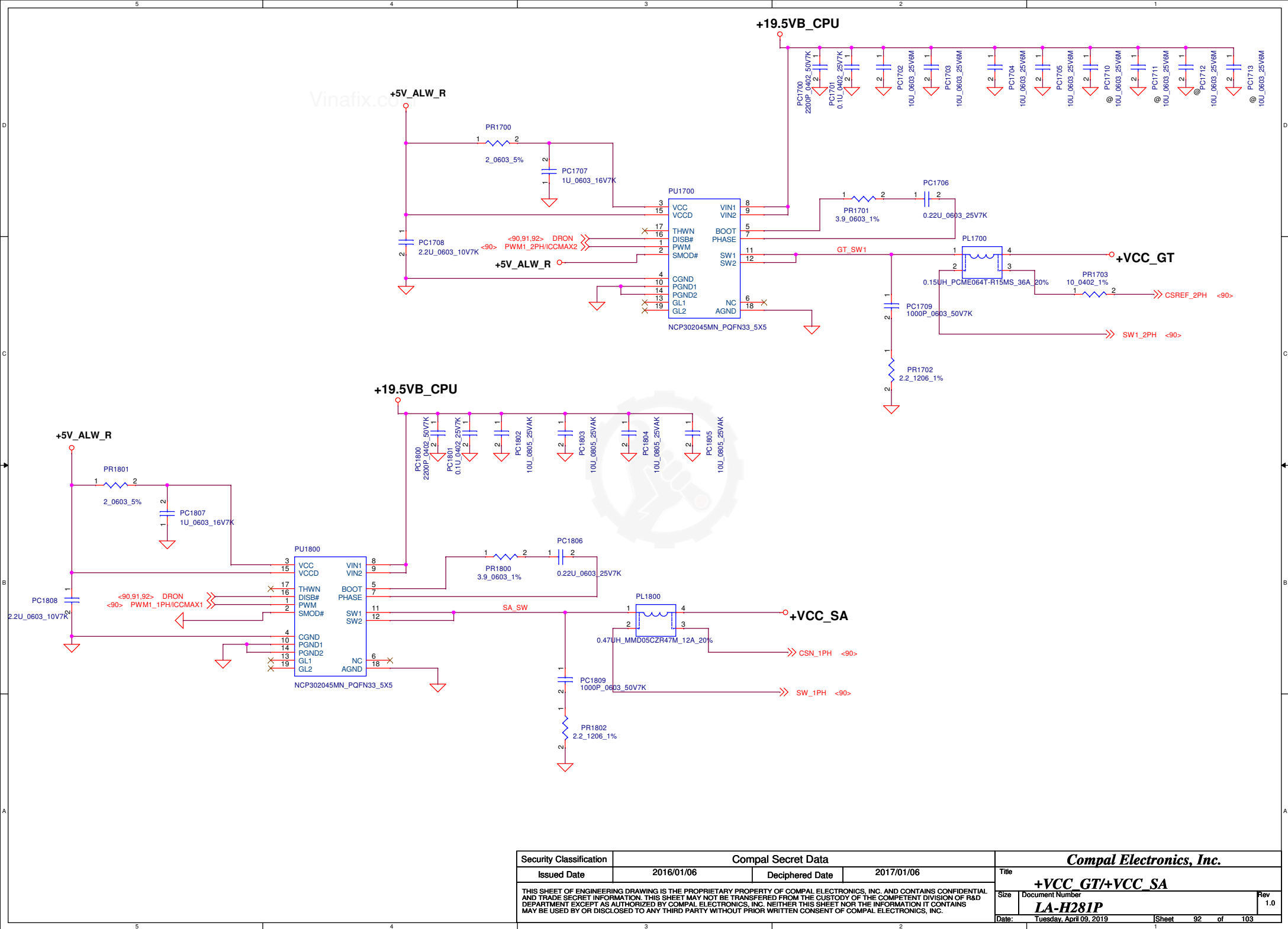


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	Compal Electronics, Inc.		
	Title		
	VCORE controller		
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+VCC_CORE

VCC_CORE
330uF X3
22uF_0603 X 22
10uF_0402 X 21
1uF_0201 X 48

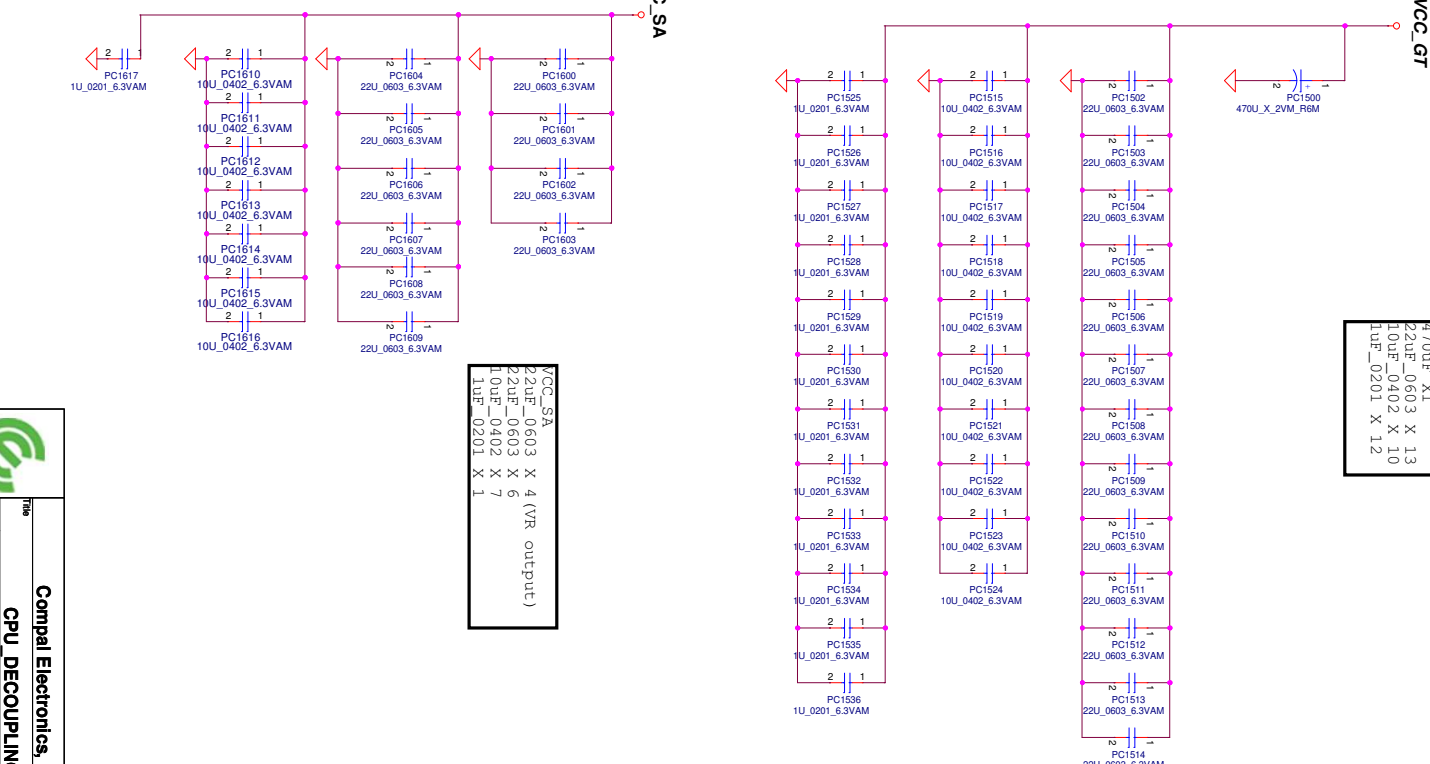
VCC_CORE (H82)
330uF X3
22uF_0603 X 28
10uF_0402 X 42
1uF_0201 X 48

+VCC_GT

VCC_GT
470uF X1
22uF_0603 X 13
10uF_0402 X 10
1uF_0201 X 12

+VCC_SA

VCC_SA
22uF_0603 X 4 (VR output)
22uF_0603 X 6
10uF_0402 X 7
1uF_0201 X 1



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Title		
BOM option component		
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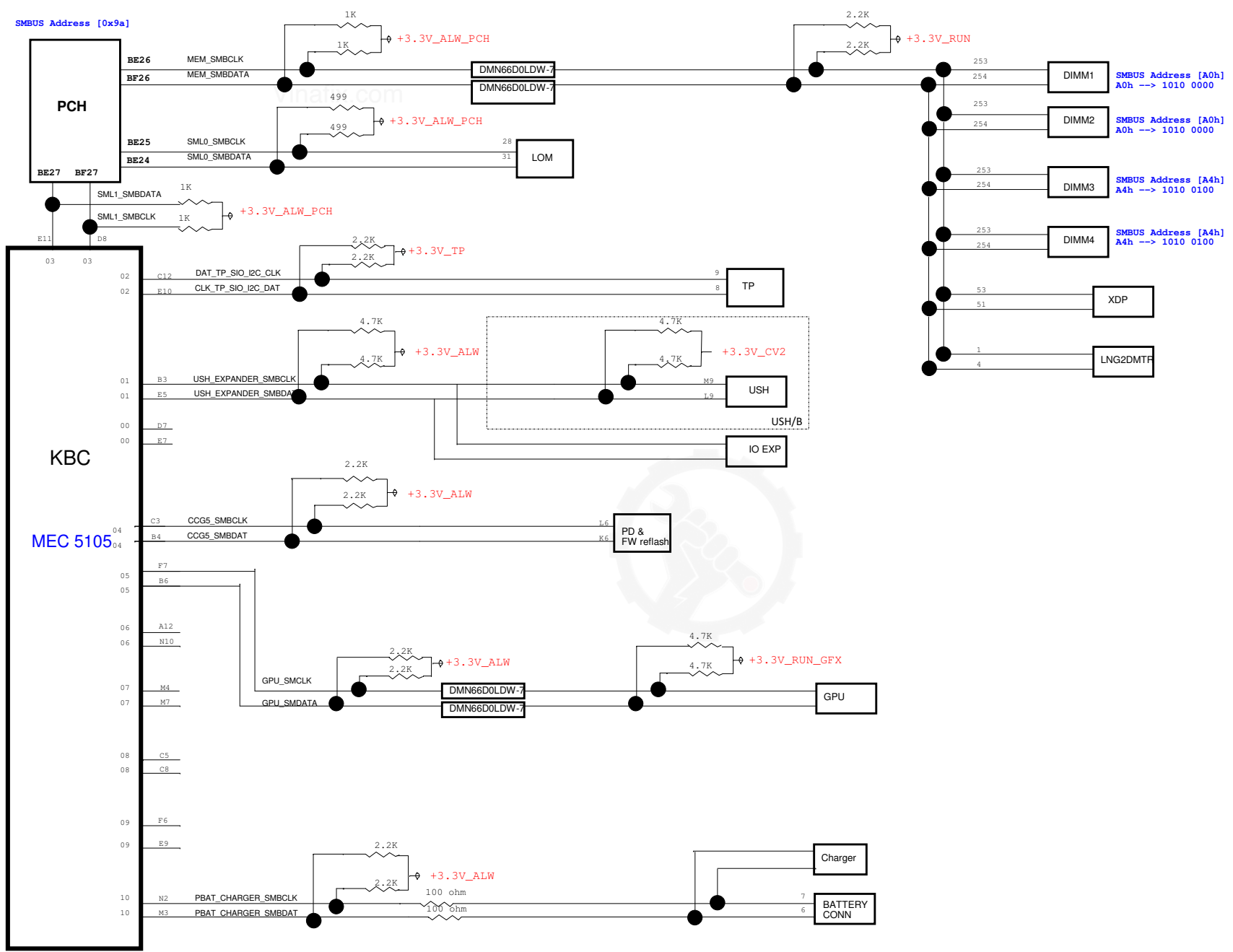
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SMBUS Address [0x9a]



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Compal Electronics, Inc.

SMBUS Block

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Version Change List (P. I. R. List)

Page 1

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	82	POWER	11/30	COMPAL	AC_DIS pull high when AC plug in to make system can't boot	Add pull down resister PR2163 to solve	0.2(X01)
2	86 87 88	POWER	11/30	COMPAL	MLCC downsize for shortage issue	PC205 change from SE000001120 to SE00000M000 PC109/PC126/PC527/PC512/PC210 change from SE025681K80 to SE074681K80	0.2(X01)
3	91	POWER	4/1	COMPAL	NCP302155 change to NCP302045 for all type CPU due to UIS package test	PU1200/PU1201/PU1202/PU1203 for H82 change from SA0000C8M00 to SA0000AOI00	1.0(A00)
4	82	POWER	4/8	COMPAL	For EMI test, need to add MLCC on +19VB path	add PC2103 SE00000G880 0.1U_0402_25V6	1.0(A00)
5		POWER		COMPAL			
6		POWER		COMPAL			
7		POWER		COMPAL			
8		POWER		COMPAL			
9		POWER		COMPAL			
10		POWER		COMPAL			
11		POWER		COMPAL			
12		POWER		COMPAL			
13		POWER		COMPAL			
14		POWER		COMPAL			
15		POWER		COMPAL			

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			Compal Electronics, Inc.	
Title		PWR_PIR		
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Item	Page#	Title	Date	Request	Owner	Issue Description	Solution Description	Rev.
1	56	EE	2018/10/2	Compal	Fix CA232 no function	CA29 and CA232 are parallel, and connector to UA1.23		0.2 (X01)
2	10	EE	2018/10/2	Compal	FOLLOW PDG V1P8 P.616 downsize from 0603 to 0402	CC185 change to 0402		0.2 (X01)
3	44	EE	2018/10/2	Compal	FRS_ON_P1 and FRS_ON_P2 have a spike to turn on 5V VBUS when CCG5 get power.	RT617,RT618 change to pop		0.2 (X01)
4	43	EE	2018/10/12	Compal	Correct downsize error	RT542,RT547 change footprint from 0402 to 0805		0.2 (X01)
5	31	EE	2018/10/12	Compal	PS8461QFN66GTR-A0 change to A4	UV66,UV67		0.2 (X01)
6	58	EE	2018/10/12	Compal	MEC5105 change CPN to SA00009GL30	UE1		0.2 (X01)
7	18,38,52,58	EE	2018/10/12	Compal	Change CPN from SB00000ZU00 to SB000000PV00	QE2,QH4,QV23,QZ17,QZ18		0.2 (X01)
8	77	EE	2018/10/12	Compal	Correct error	H20,H23 Change to NPTH		0.2 (X01)
9	42	EE	2018/11/27	Compal	Place holder for future VBUS-short fix (reduce current surge) (align Northbay)	Reserve RT621,RT622 0 ohm		0.2 (X01)
10	21	EE	2018/11/27	Compal	Align Northbay pop LH423,CH560,CH324	RH289 change LH423, CH324 change to pop, Add CH560		0.2 (X01)
11	77	EE	2018/11/27	Compal	Update JKBTP1,JLED1,JPB1 symbol	JKBTP1,JLED1,JPB1		0.2 (X01)
12	10	EE	2018/11/30	Compal	Change LC562 from 0_0603_5% to Beads Align BH	RC422 change to LC562		0.2 (X01)
13	45	EE	2018/12/4	Compal	Material Shortage.	DT2001~DT2008 change to SCS00000F200 from SCS000000X00		0.2 (X01)
14	42	EE	2018/12/5	Compal	Support vpro on docking side reserve	Add RT623,RT624		0.2 (X01)
15	58,59	EE	2018/12/7	Compal	Correct RTD3_SELECT to right GPIO	Change RTD3_SELECT to UE12.21 from UE1.E1.Add RE750 to UE1.E1 for UE1.E1 no use.		0.2 (X01)
16	38,59	EE	2018/12/7	Compal	Reserve GPIO pins for DID2.0 feature	Add Net "DID2_GPIO1,DID2_GPIO2"		0.2 (X01)
17	65	EE	2019/1/15	Compal	TPM ES Chip change to MP(QS) part(UZ12)	Change to SA0000AQ270		0.2 (X01)
18	77	EE	2019/1/15	Compal	CLIP1,CLIP2	Change to @RF@		0.2 (X01)
19	62	EE	2019/1/15	Compal	Board ID	Change to 62Kohm		0.2 (X01)
20	45	EE	2019/1/15	Compal	DT2001~DT2008 shortage	Change to SCS00000F800		0.2 (X01)
21	58	EE	2019/1/15	Compal	TBT_RESET_N_EC (RE506)	Change to pop		0.2 (X01)
22	59,22,20,58,38,22,38	EE	2019/1/15	Compal	Before DVT1.0,PPM feedback material shortage(RD check ok for install material) SB000002R00 change to SB000013V00 SB000000J500 change to SB000010O00 SB000000QP00 change to SB000000T900 SB000010C00 change to SB000008S80	QE4, QZ20, QH7, QE15, QV8, QZ1 QV1		0.2 (X01)
23	51	EE	2019/1/15	Compal	LAN IEEE EA change to 0ohm (RL71~RL78)	Change to SD028000080		0.2 (X01)
24	44	EE	2019/1/15	Compal	TYPE C AUX change to 0ohm (CT385~CT388)	Change to SD043000080		0.2 (X01)
25	59	EE	2019/1/15	Compal	UE12 USE DVT1.0 CPN : SA00009YF10 and apply new symbol	Change to SA00009YF10		0.2 (X01)
26	56	EE	2019/1/21	Compal	Change BOM Structure to EMI@	CA224 CA225		0.2 (X01)
27	59	EE	2019/1/18	Compal	Board ID(DVT1.1) (RE79)	Change to 33Kohm		0.3 (X02)
28	38	EE	2019/1/18	Compal	Fuse change to one time used (FV1)	T0603FF1500TM (17")		0.3 (X02)
29	38	EE	2019/1/21	Compal	BL_PWR_SRC & LCDVDD monitor	RV907 change to 4.3M, RV908 change to 1.2M		0.3 (X02)
30	71	EE	2019/1/21	Compal	DI3 17" follow 15" CPN for X1 code	Change to SCA00000T00		0.3 (X02)
31	38	EE	2019/1/21	Compal	Align NB reserve fuse FZ3, FZ4 and netname	Change to T0603FF1000TM		0.3 (X02)
32	19	EE	2019/1/21	Compal	Align BH GPIO TYPEC_CON_SEL1 / TYPEC_CON_SEL2	RH553~RH556		0.3 (X02)
33	38	EE	2019/1/24	Compal	Add RV911 for pull down float voltage	RV911		0.3 (X02)
34	45	EE	2019/1/24	Compal	Change BOM Structure to EE	DT1, DT2, DT3,DT16, DT2001~DT2008		0.3 (X02)
35	59	EE	2019/1/25	Compal	DI6 change CPN	Change to SC300001Y00		0.3 (X02)
36	38	EE	2019/1/29	Compal	Update UE12 symbol	Change to SA00009YF10		0.3 (X02)
37	27,38	EE	2019/1/29	Compal	HDR monitor for AMD/NV/UMA edp output detect	RV737~742, QV44		0.3 (X02)
38	38	EE	2019/1/30	Compal	Change the power rail to +3.3V_RUN	RV739,RV740		0.3 (X02)
39	38	EE	2019/1/31	Compal	Change net name from +CAMERA_VDD_F to +CAMERA_VDD	CZ510, CZ511, CZ512		0.3 (X02)
40	42	EE	2019/2/12	Compal	Change to depop, Change BOM Structure to @	RT372		0.3 (X02)
41	42	EE	2019/2/12	Compal	Change BOM Structure	RT614		0.3 (X02)
42	27	EE	2019/2/21	Compal	Cancel double pull high	RV806		0.3 (X02)

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